

ZZZ PCB@

B 252 LA-F251P REV0 M/B 1
DA8001BW010

Vinafix.com

UC1 KBL_U42_I7_QS18@



S IC A31 FJ8067703281816 QNBF Y0 1.8G
SA0000AWC0L

UC1 KBL_U42_I5_QS16@



S IC A31 FJ8067703282221 QNEG Y0 1.6G
SA0000AWB1L

UC1 KBL_U42_I7_18G@



S IC FJ8067703281816 SR3LC Y0 1.8G A31!
SA0000AWC2L

UC1 KBL_U42_I5_16G@



S IC FJ8067703282221 SR3LB Y0 1.6G A31!
SA0000AWB3L

UC1 KBL_U42_I7_QS19@



S IC A31 FJ8067703281718 QNBE Y0 1.9G
SA0000AWR0L

UC1 KBL_U42_I5_QS17@



S IC A31 FJ8067703282016 QNEE Y0 1.7G
SA0000AWS0L

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DDH40 / DDH50 MB Schematic Document

LA-F251P

Rev: 1.0

2017.07.24

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Title

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Size

Document Number

Rev

LA-F251P

1.0

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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF

PM TABLE

power plane State	+RTC_CELL +RTC_VCC +3VLP +19VB	+1.0V_PRIM +1.0V_MPHYPLL +5VALW +3VALW +3.3V_ALW_DSW +1.8V_PRIM	+1.0V_VCCST +1.2V_DDR +2.5V_MEM +3VALW_PCH	+1.0VS_VCCIO +1.0V_VCCSTG +VCC_GT +VCC_SA +VCC_CORE +GPU_CORE +5VS +3VS +0.6V_DDR_VTT
S0	ON	ON	ON	ON
S3	ON	ON	ON	OFF
S4&S5 / AC	ON	ON	OFF	OFF
S4&S5 / DC	ON	OFF	OFF	OFF

Board ID & Model ID table

Item	Pull-down(K ohm)	Pull-up (K ohm)	Voltage	Board ID/Model ID
1	100	10.0	3.000	EVT(X00)
2	100	13.7	2.902	
3	100	17.8	2.801	DVT1(X01)
4	100	22.1	2.703	
5	100	27.0	2.598	DVT2(X02)
6	100	32.4	2.492	
7	100	37.4	2.402	
8	100	49.9	2.201	Pilot(A00)
9	100	57.6	2.094	
10	100	64.9	2.001	
11	100	73.2	1.905	
12	100	82.5	1.808	
13	100	93.1	1.709	
14	100	107.0	1.594	

USB PORT#	DESTINATION
1	USB3.0 Port0
2	USB3.0 Port1
3	USB3.0 Port2 (IO Board)
4	USB2.0 Port0
5	HD CAM
6	Card Reader
7	BT
8	Touch Screen
9	Finger Printer
10	N/A

USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				USB3.0 Port0
USB3.0-2	SSIC-1			USB3.0 Port1
USB3.0-3	SSIC-2			USB3.0 Port2 (IO Board)
USB3.0-4				N/A
USB3.0-5		PCIE-1		GPU
USB3.0-6		PCIE-2		GPU
		PCIE-3		GPU
		PCIE-4		GPU
		PCIE-5		GLAN
		PCIE-6		WLAN
		PCIE-7	SATA-0	SATA HDD
		PCIE-8	SATA-1	N/A
		PCIE-9		SSD
		PCIE-10		SSD
		PCIE-11	SATA-1*	SSD
		PCIE-12	SATA-2	SSD

CPU PWR
GPU PWR
Peripheral Device PWR

ADAPTER

CHARGER
ISL8739HRZ-T
(PU703)

BATTERY

+PWR_SRC
(+19VB)

RT8207PGQW
(PU200)

+1.2VP
+1.2V_DDR
+0.6VSP
+0.6V_DDR_VTT

+1VALWP
+1.0V_PRIM

+DCBATOUT_LCD
+IR_LED+

+1.35VGPUP
+1.35VS_VRAM

+5VALWP
+5VALW

+VL
+USB30_VCCA
+USB30_VCCB
+USB30_VCCC
+5VS

+TP_VDD
+3VS
+3VALW_PCH
+3V_VA

+1.8VALWP
+1.8V_PRIM
+2.5VP
+2.5V_MEM

+1.0V_VCCSTG_C
+1.0V_MPHYPLL
+1.0V_VCCST
+1.0VS_DGPU

+1.0VS_VCCIO
+1.0V_VCCSTG

+TPAN_VDD
+5V_HDD
+5VS_HDMI
+5V_KB_BL

+LCDVDD
+3.3V_LAN
+3.3V_WLAN
+3.3V_CAM
+3VS_SSD

+3VS_1.8VS_DGPU_MAIN
+3VS_1.8VS_DGPU_AON
+CPVDD
+1.8V_AVDD

+VCC_SA
+VCC_CORE
+VCC_CORE
+VCC_GT
+GPU_CORE
+VCC_CORE_42
+VCC_GT_42

+RTC_CELL
+RTC_VCC

+3VALWP
+3VALW

+3VLP
+3VALW

+3VALW
+3VALW

+3VALW
+3VALW

NCP81253
(PUA01)
AON7934
(PQA01)

NCP302035
(PUI01)

NCP302035
(PUI02)

NCP302035
(PUG01)

RT8816AGQW
(PU1101)

00hm 0805
(PRC01)

00hm 0805
(PRC03)

00hm 0805
(PRC02)

BAS40C
(D2501)

TPS2544RTER
(UUS5)

AP22802BW5
(U3504)

AP22802BW5
(U3505)

EM5209VF
(U22)

NTK3139PT1G
(Q6203)

EM5209VF
(U22)

00hm 0603
(RZ1705)

00hm 0402
(RC1124)

RT8061AZQW
(PU500)

RT9059GSP
(PU800)

RT9724GB
(U5201)

SY6288C20AAC
(UL3)

00hm 0805
(R5809)

00hm 0603
(R5229)

+VCC_SA

+VCC_CORE

+VCC_CORE

+VCC_GT

+GPU_CORE

+VCC_CORE_42

+VCC_GT_42

+RTC_CELL

+RTC_VCC

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+3VALW

+3VLP

+3VALW

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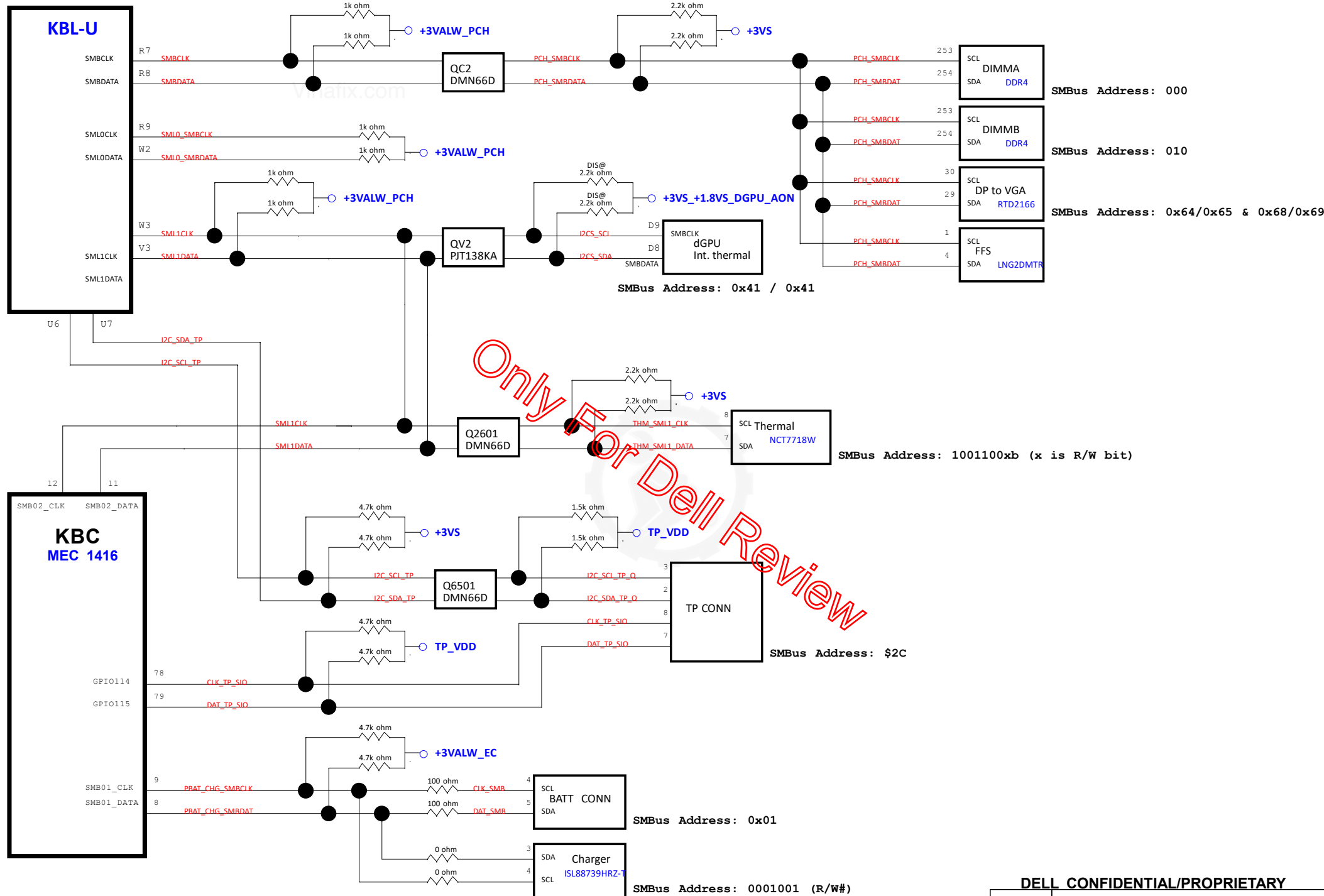
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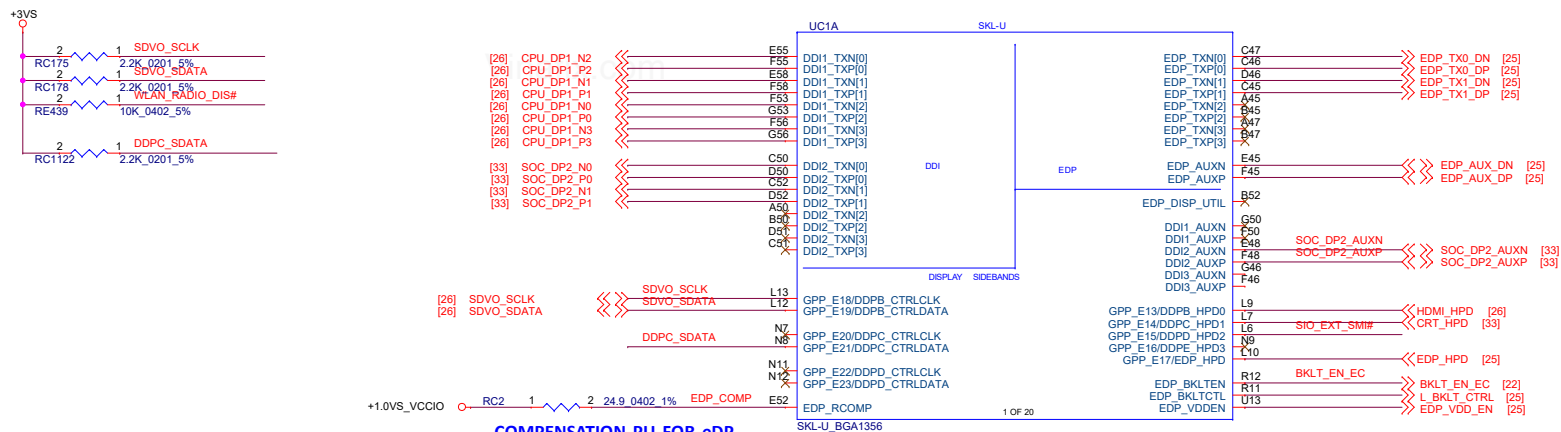
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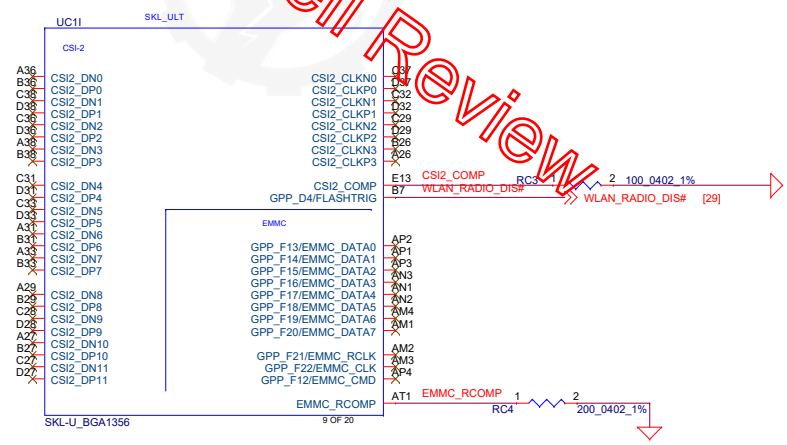
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Power rails			
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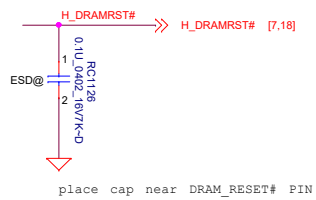
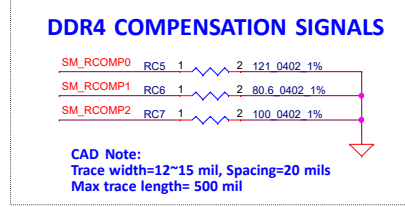
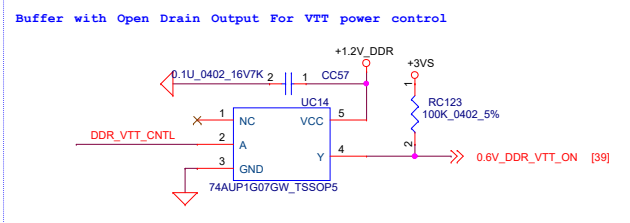
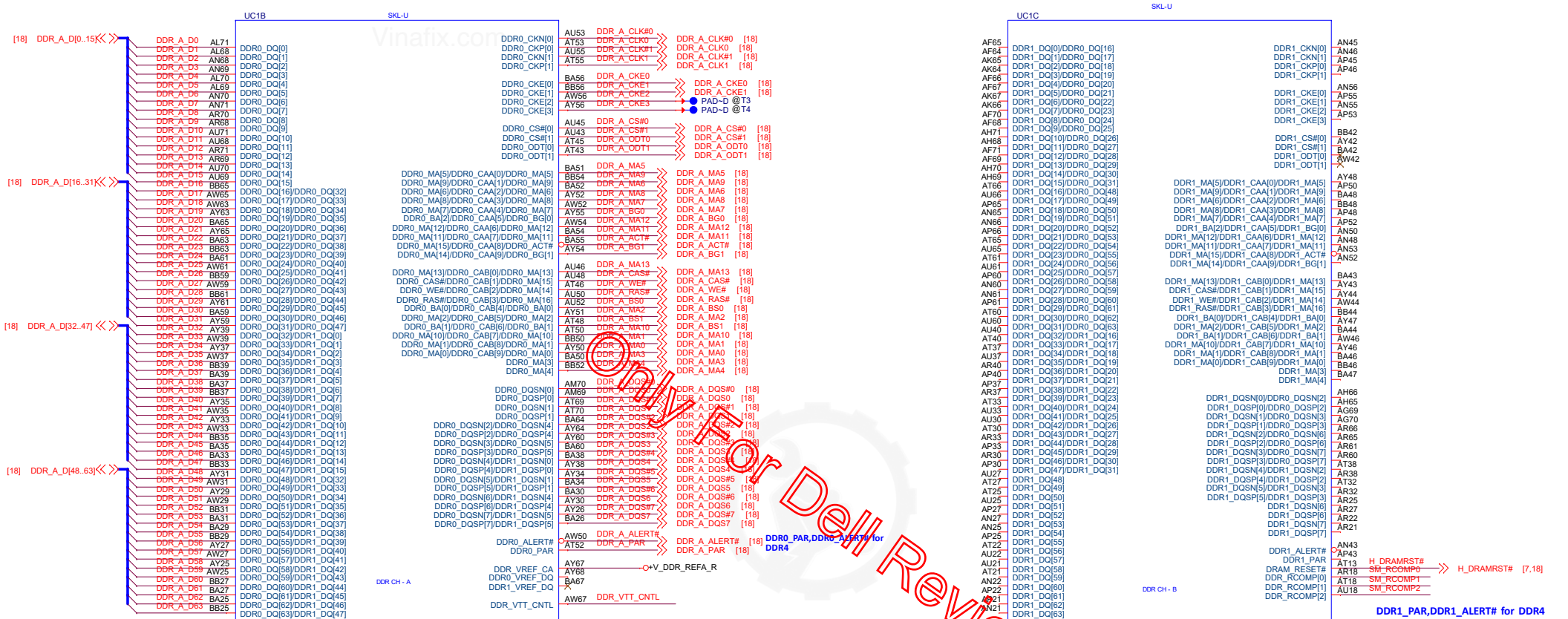
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DDR4, Ballout for B2B(Interleave)



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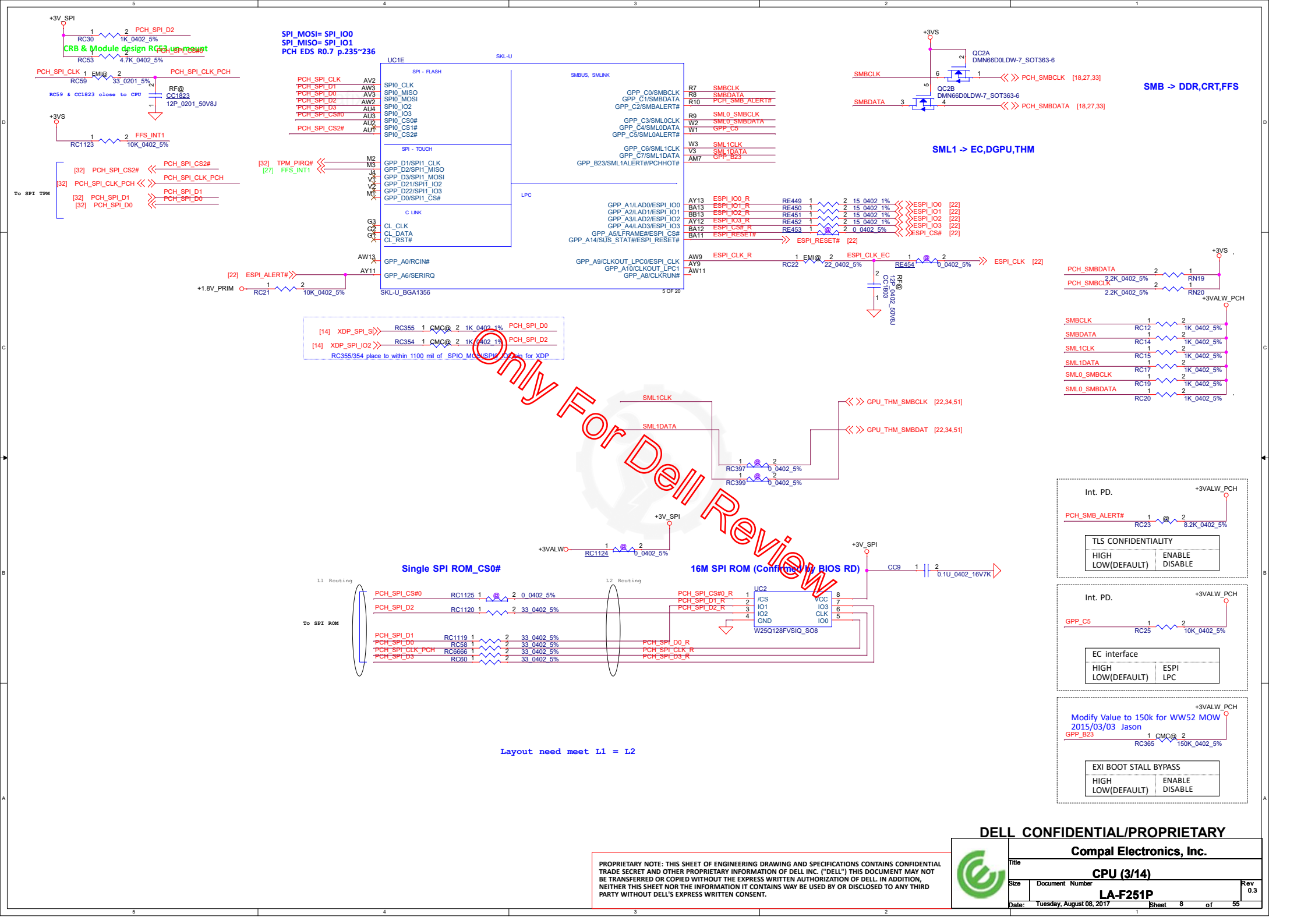
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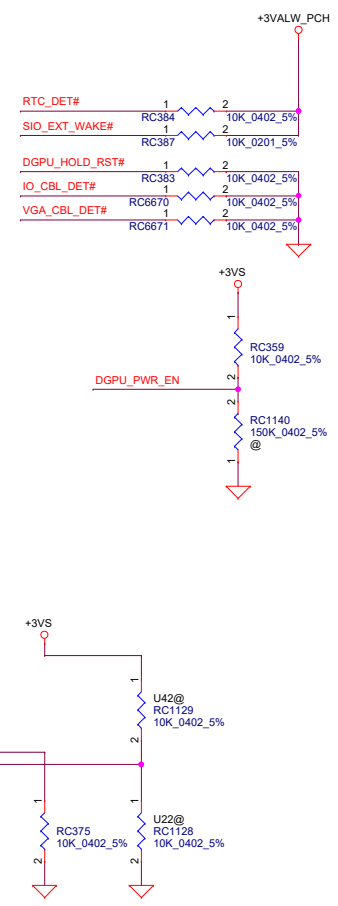
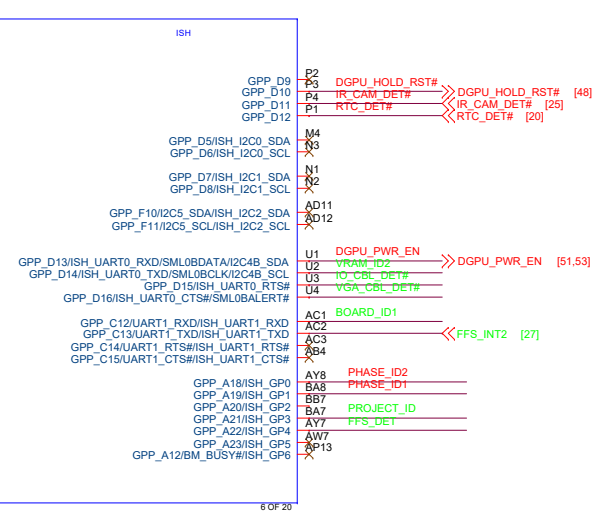
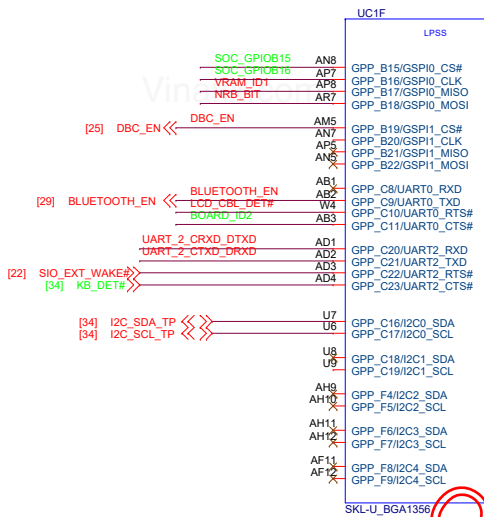
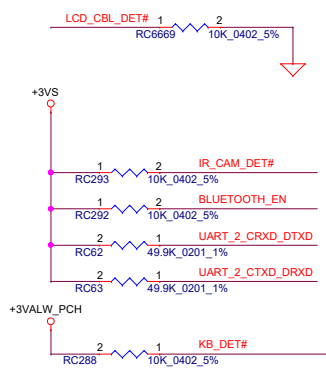
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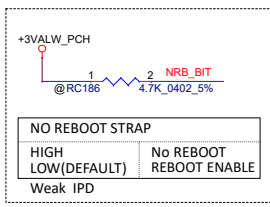
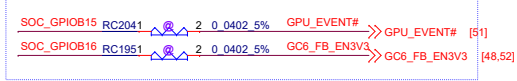
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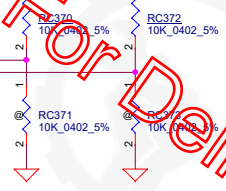
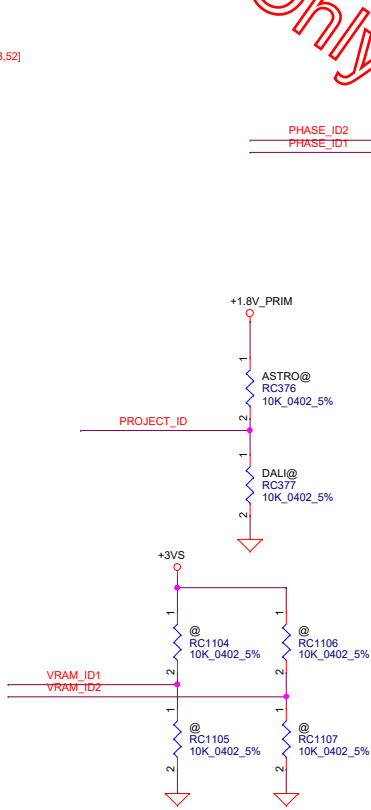
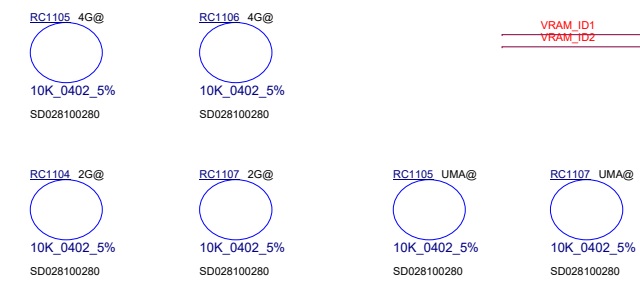
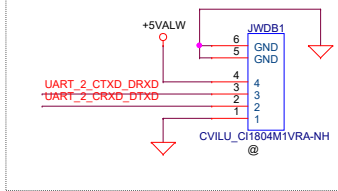


TO DGPU



Win7 Debug solution

Option 2 : For Open Chassis Platforms



PHASE ID	PHASE_ID1 (GPP_A19)	PHASE_ID2 (GPP_A18)
EVT	0	0
DVT1	0	1
DVT2	1	0
Pilot	1	1

PROJECT ID	PROJECT_ID (GPP_A21)
Dali	0
Astro	1

BOARD ID	BOARD_ID1 (GPP_C12)
KBL-U	0
KBL_RU	1

BOARD ID	BOARD_ID2 (GPP_C11)
	0

VRAM ID (PCBA VRAM Size Config.)	VRAM_ID2 (GPP_D14)	VRAM_ID1 (GPP_B17)
UMA	0	0
2G	0	1
4G	1	0
AMD	1	1

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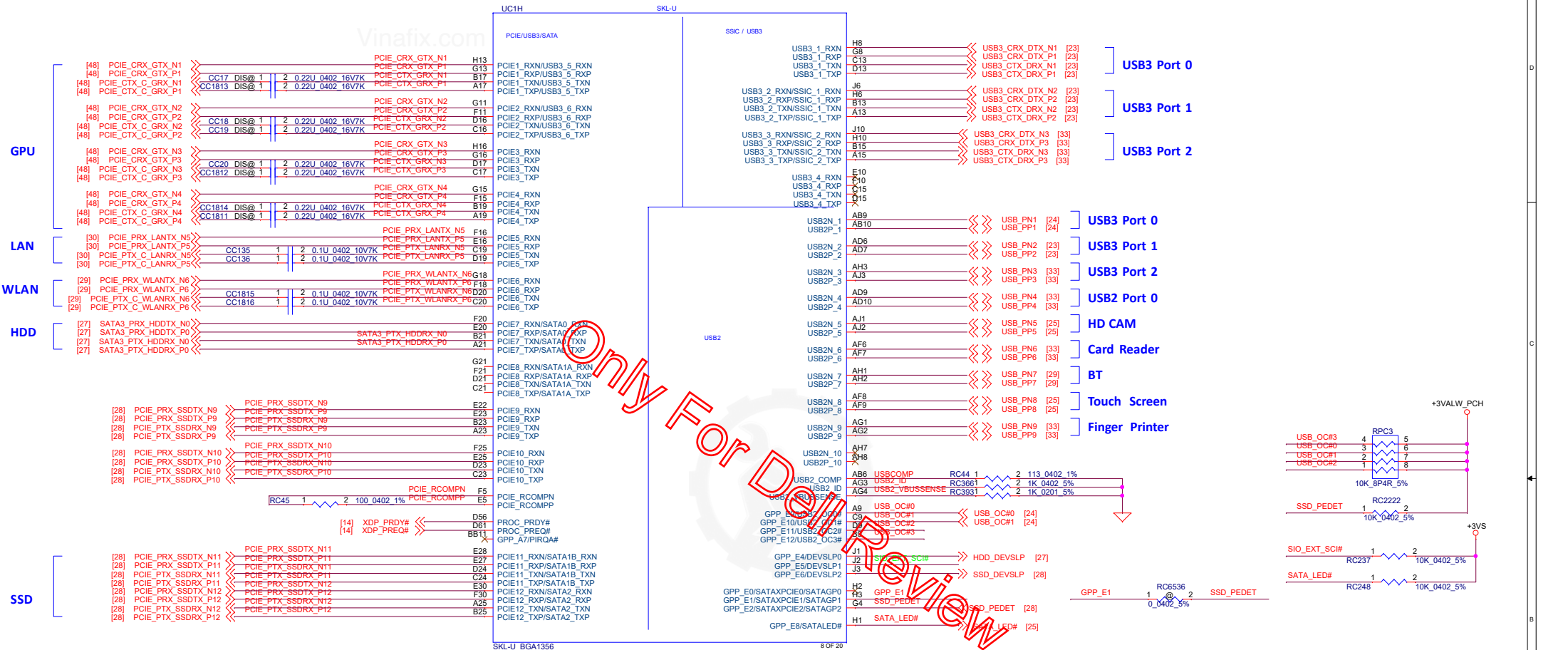
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CPU (4/14)

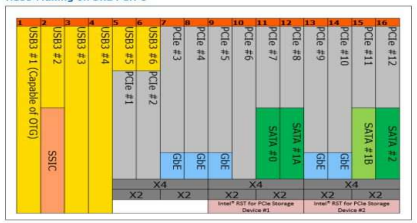
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3.4.1 SKL PCH U Flexible I/O
Figure 3-1. HSIO Muxing on SKL PCH U



- There are 16 HSIO lanes on SKL PCH-LP U Series, supporting the following port configurations:
- Up to 12 PCIe* lanes (multiplexed with USB 3.0 ports, SATA Ports)
 - Only a maximum of 6 PCIe* ports (or devices) can be enabled at any time.
 - Ports 1-4, Ports 5-8, and Ports 9-12, can each be individually configured as 4x1, 2x2, 1x2 + 2x1, or 1x4.
 - Up to 3 SATA Ports (multiplexed with PCIe*)
 - SATA Port 1 has the flexibility to be mapped to either PCIe* Port 8 or Port 11.
 - Up to 6 USB 3.0 ports (multiplexed with PCIe*)
 - USB Dual Role (OTG) capability is available on USB 3.0 Port 1
 - One SSIC x1 port is multiplexed with USB 3.0 Port 2
 - One GbE lane
 - GbE can be mapped into one of the PCIe* Ports 3-5 and Ports 9-10
 - When GbE is enabled, there can be at most up to 5 PCIe* ports enabled.
 - Up to 2 Intel RST for PCIe* storage devices supported
 - Devices can be x2 or x4
 - Devices can be implemented on PCIe Ports 5-8 and Ports 9-12

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

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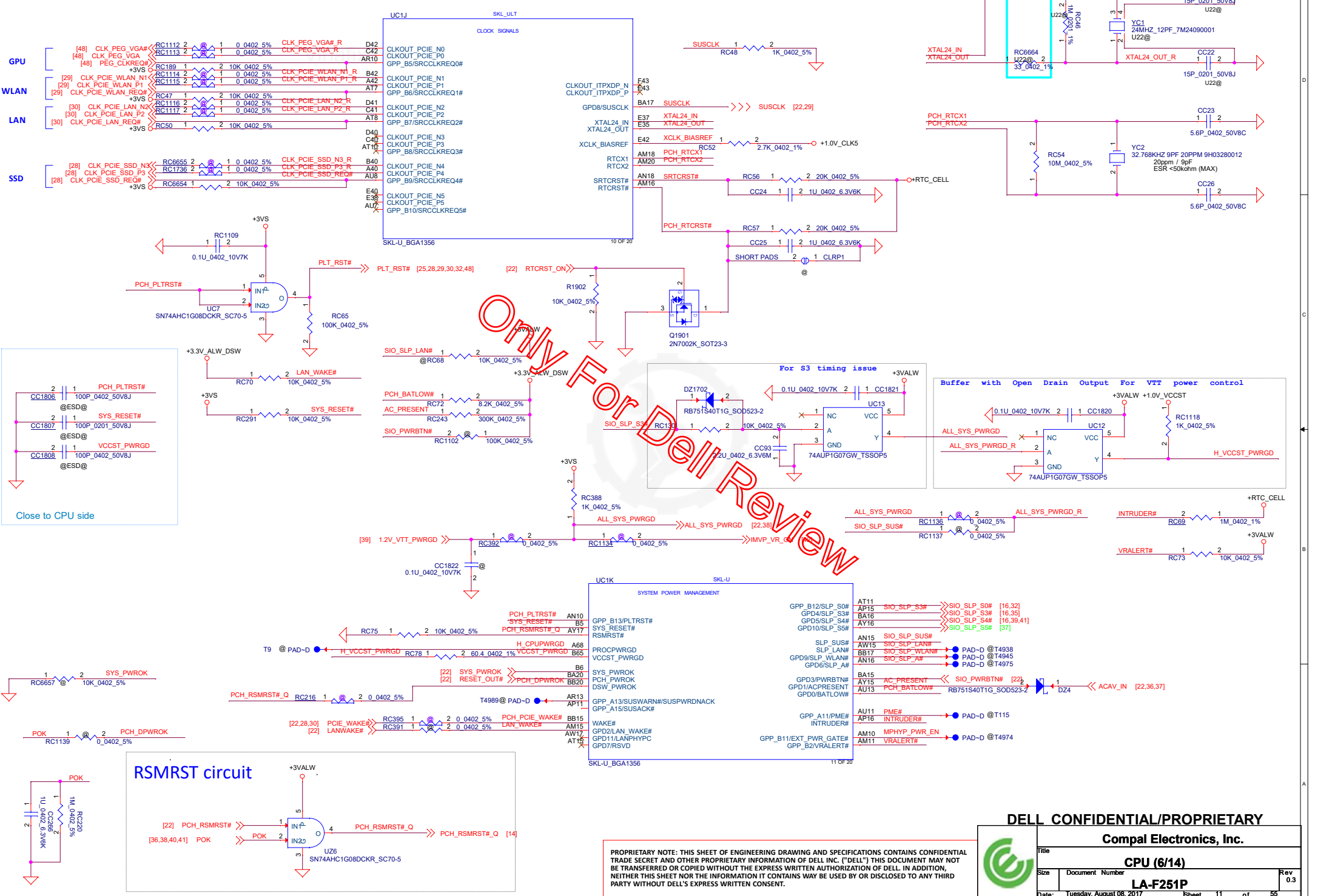
CPU (5/14)

LA-F251P

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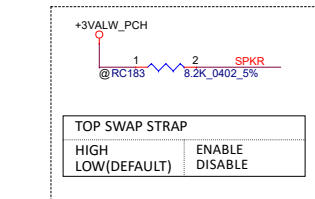
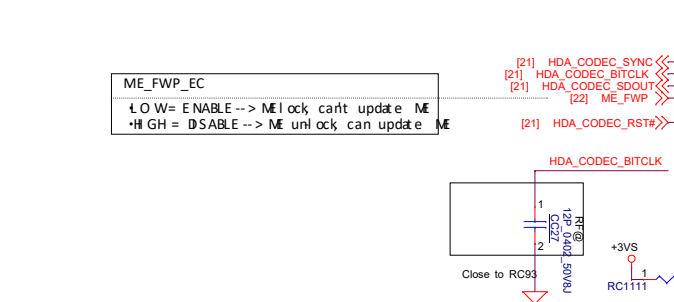
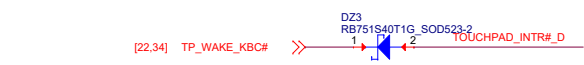
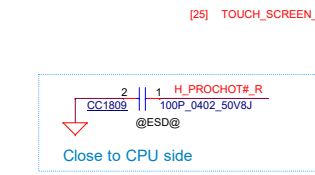
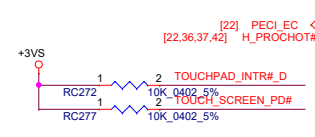
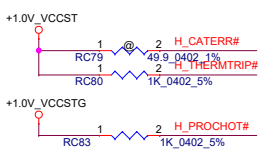
EMI check on EVT



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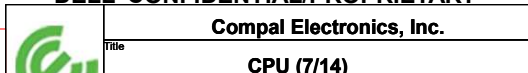
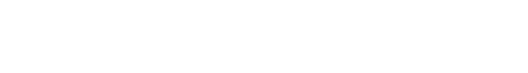
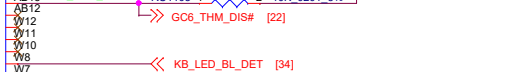
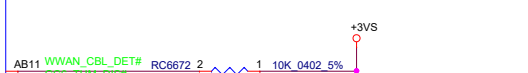
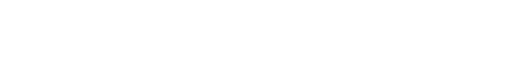
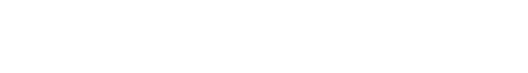
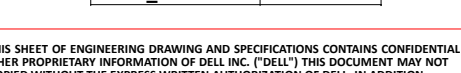
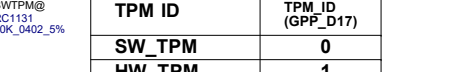
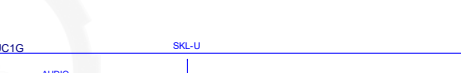
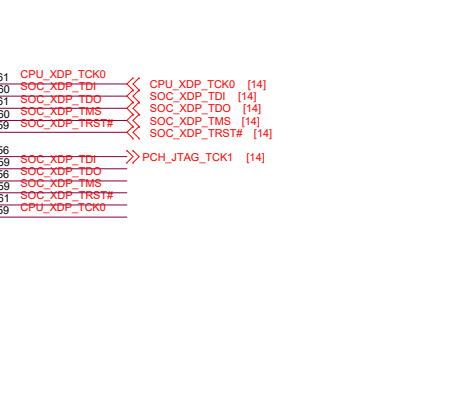
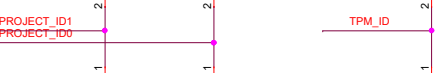
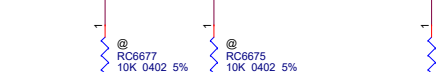
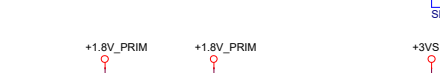
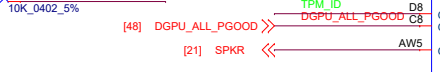
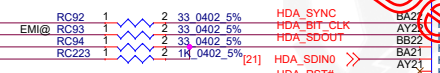
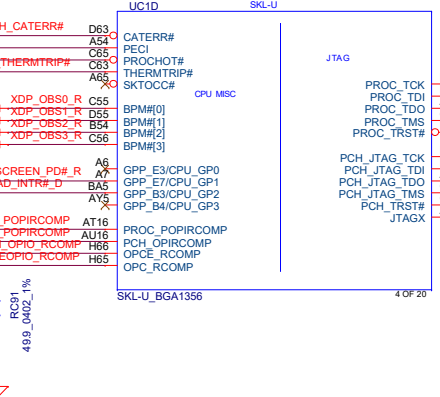
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Compal Electronics, Inc.		
CPU (6/14)		
Size	Document Number	Rev
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TOP SWAP STRAP	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

Flash Descriptor Security override	
HIGH	DISABLE
LOW(DEFAULT)	ENABLE

PROJECT ID	PROJECT_ID1 (GPP_F1)	PROJECT_ID2 (GPP_F0)



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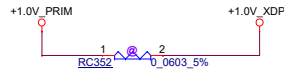
Compal Electronics, Inc.

CPU (7/14)

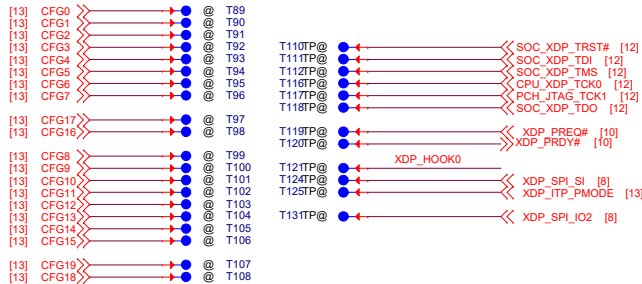
LA-F251P

Date: Tuesday, August 08, 2017 Sheet 12 of 55

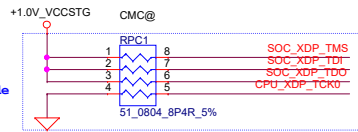
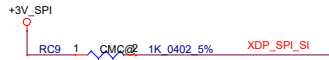
PRIMARY CMC CONN



Vinafix.com



[11] PCH_RSMRST#_Q >> PCH_RSMRST#_Q RC1581 CMC@ 2 1K 0402 5% XDP_HOOK0



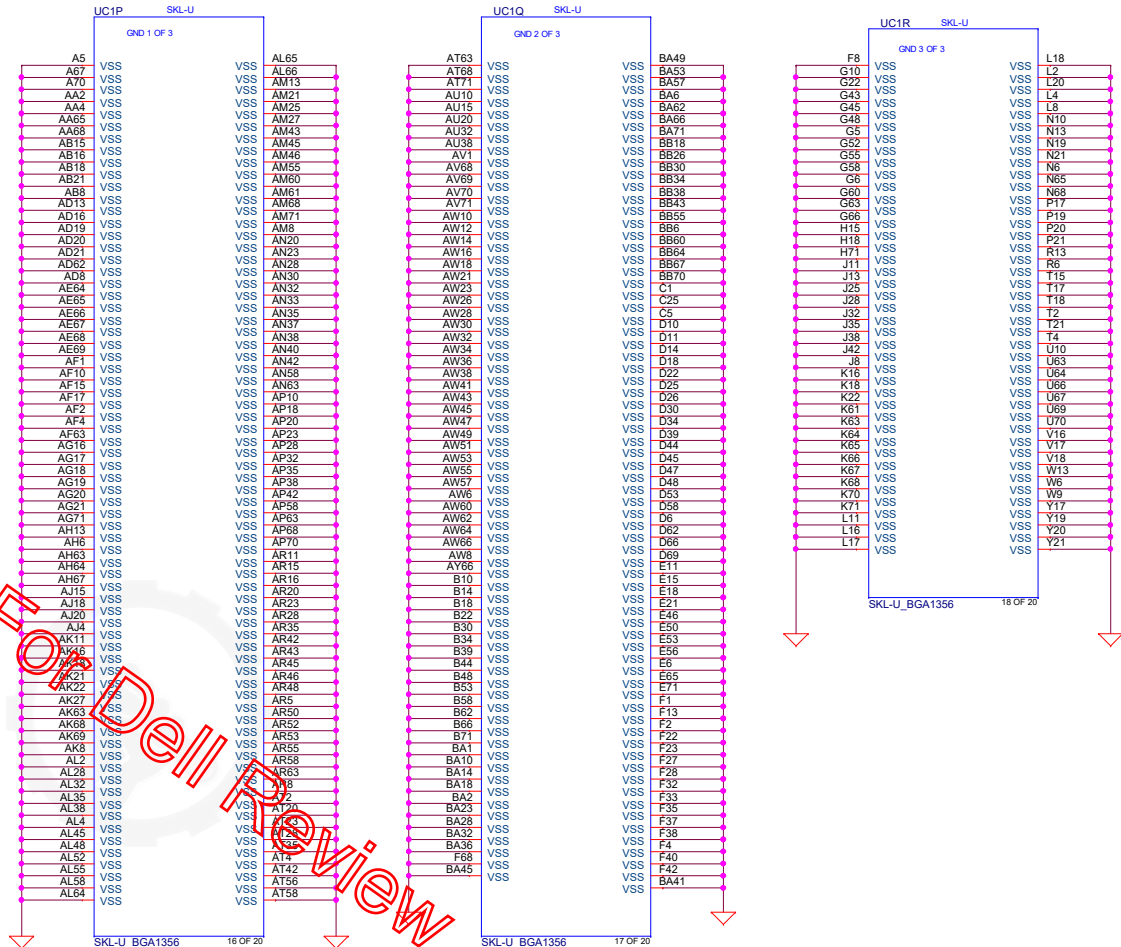
Place to CPU side



Place to CPU side



XDP_SPI_I02 = XDP_PRSENT_PCH
CFG3 = XDP_PRSENT_CPU



For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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Title CPU (9/14)			
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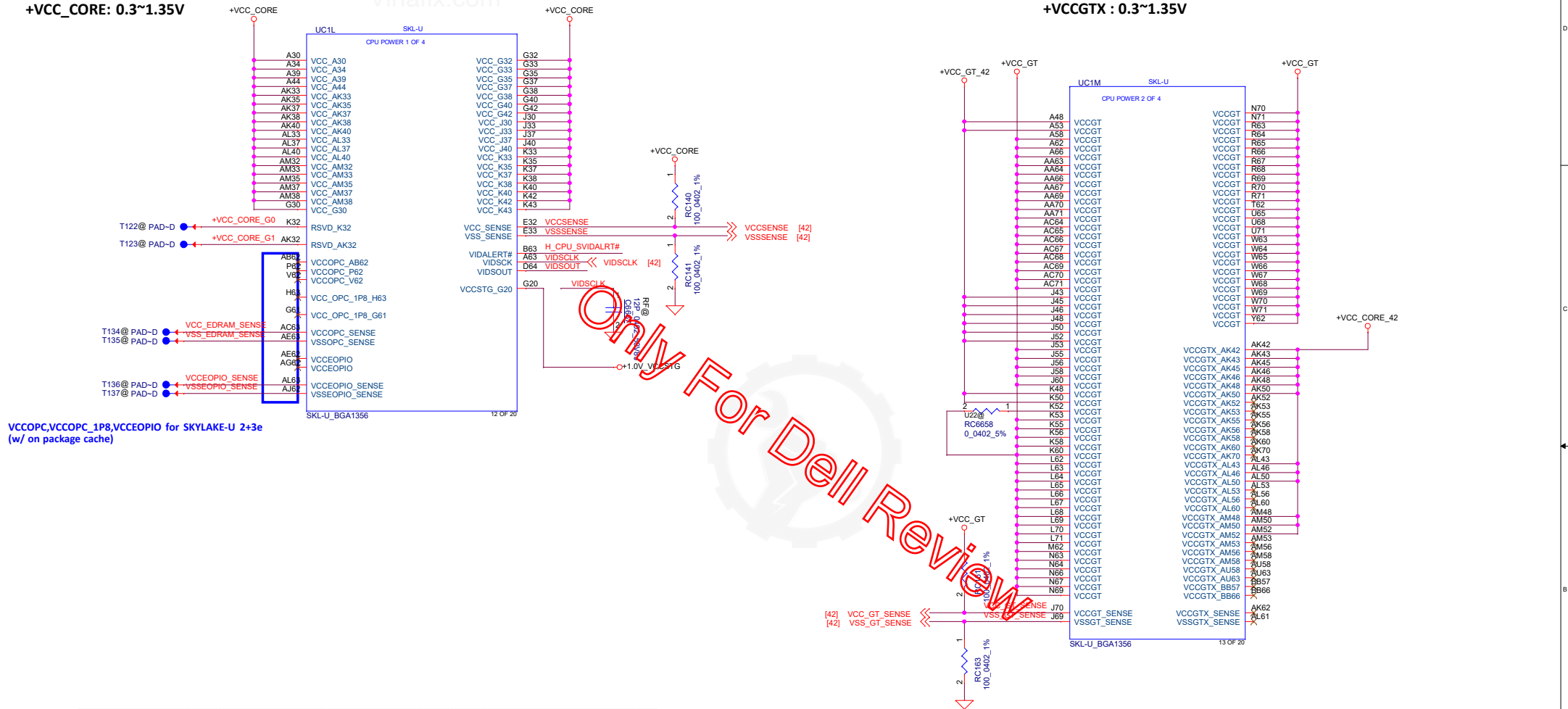
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PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

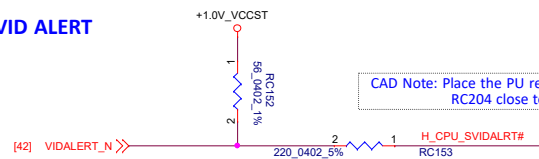
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC_CORE: 0.3~1.35V

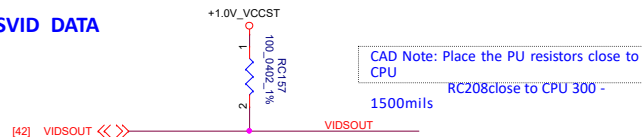
+VCCGT: 0.3~1.35V
+VCCGTx: 0.3~1.35V



SVID ALERT



SVID DATA

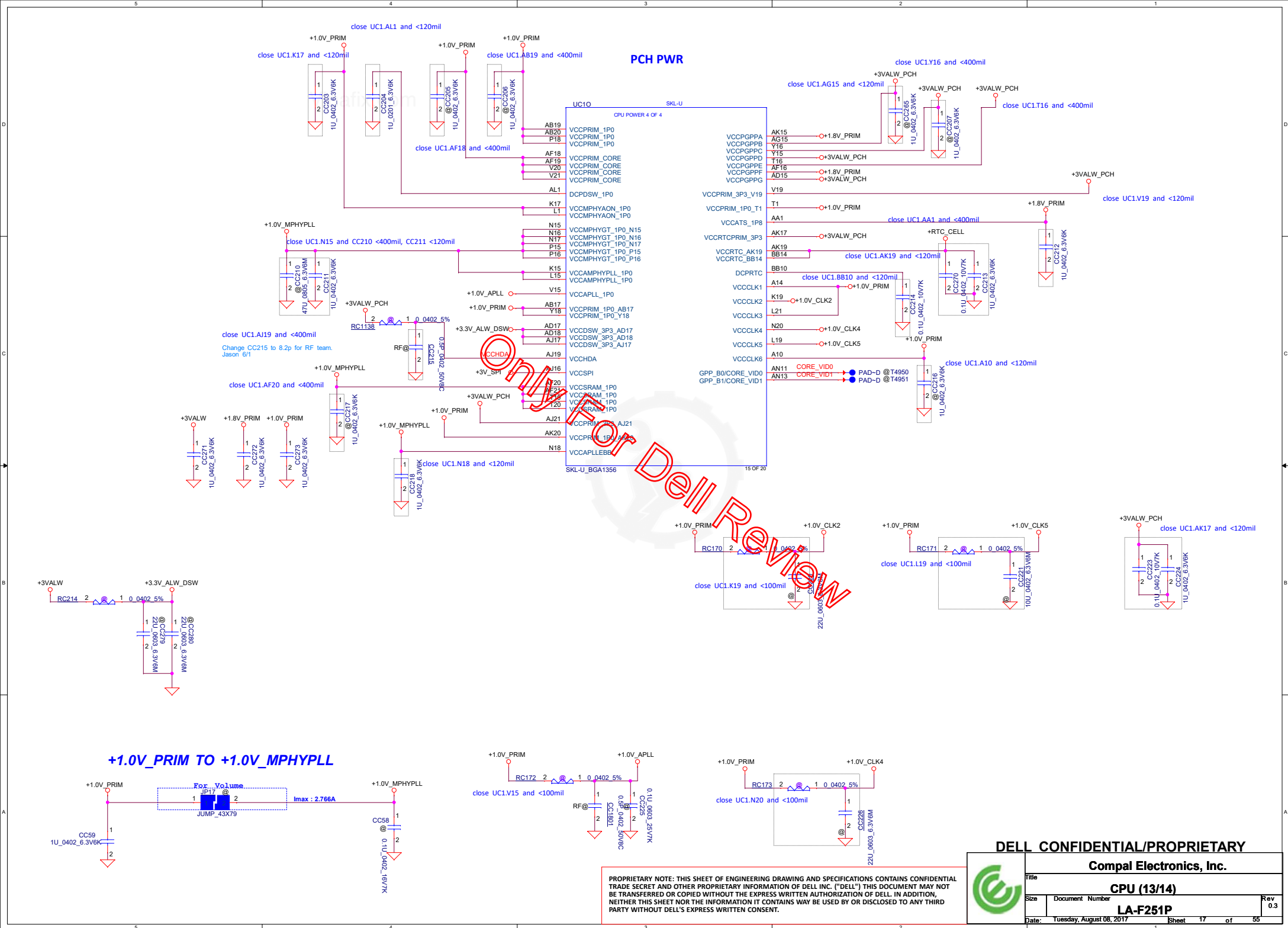


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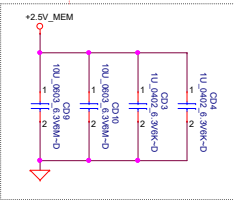
DELL CONFIDENTIAL/PROPRIETARY



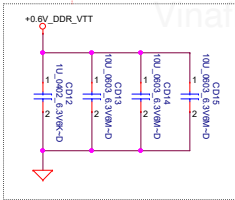
Compal Electronics, Inc.			
CPU (10/14)			
Size	Document Number	Rev	
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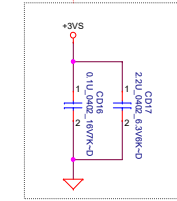
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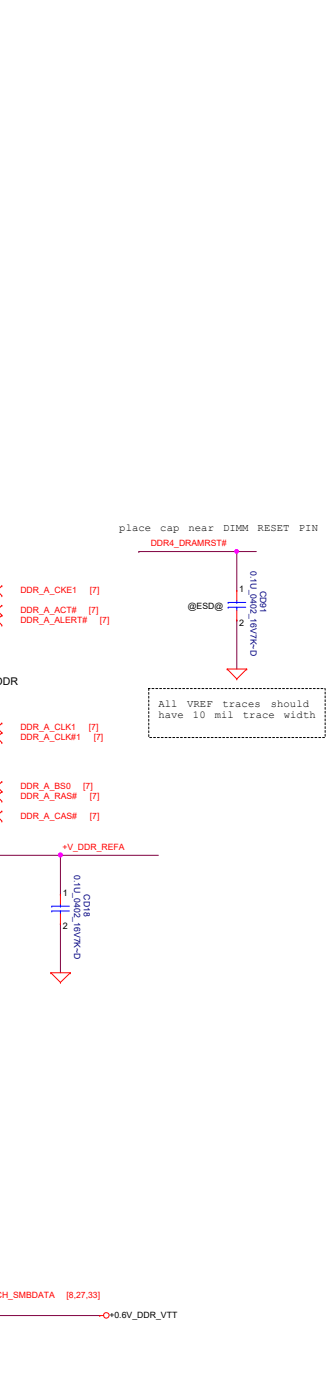
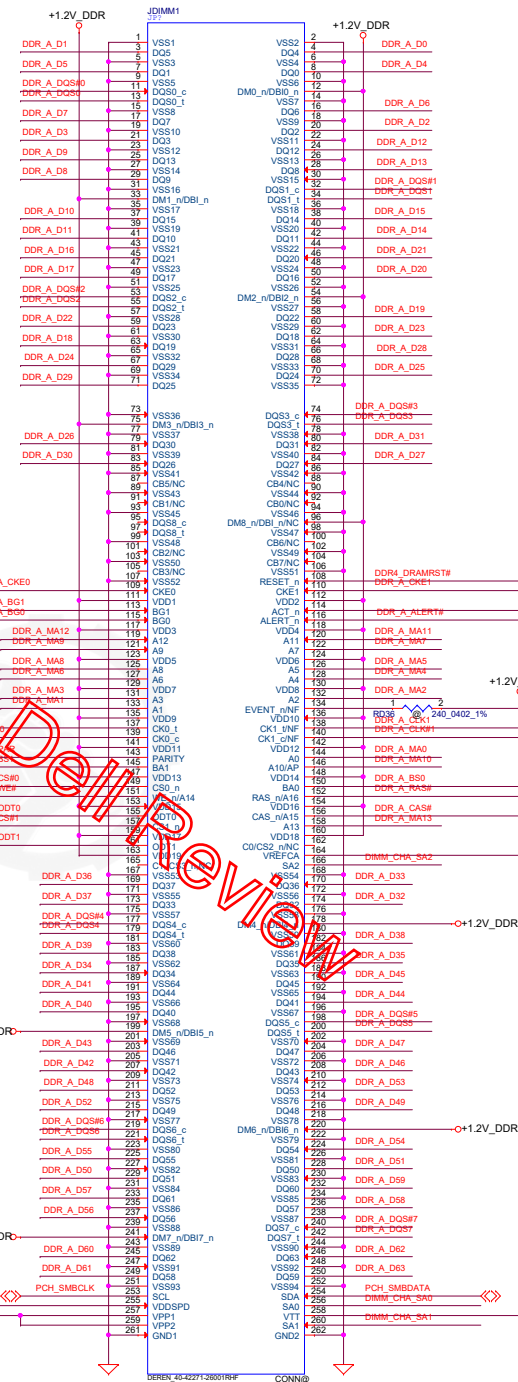
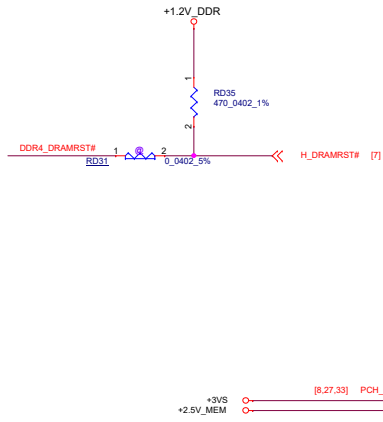
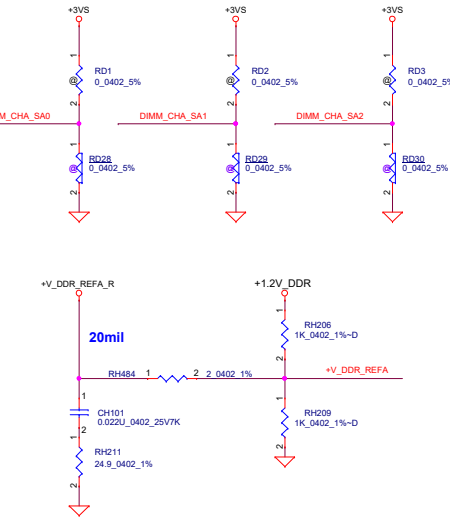
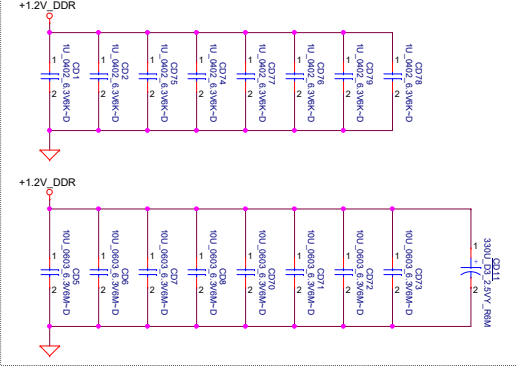
Layout Note:
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Layout Note:
Place near JDIMM1.255



Layout Note:
Place near JDIMM1

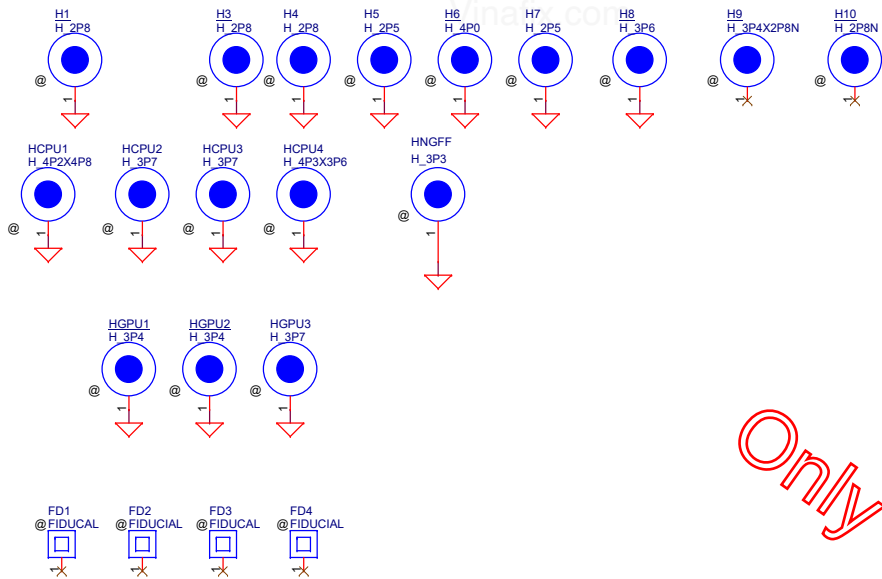


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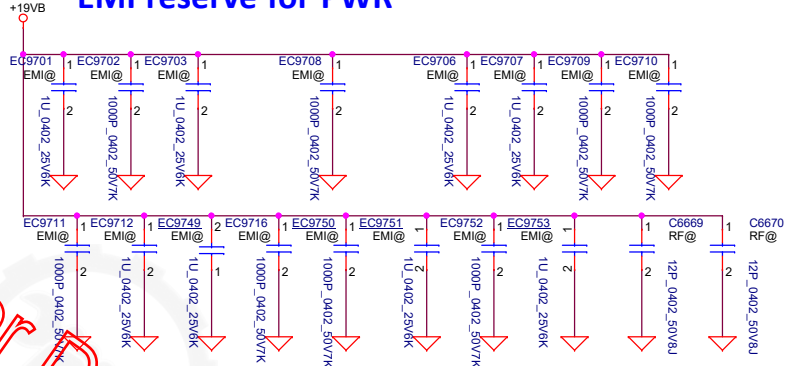
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Issued Date	2015/01/30	Deciphered Date	2016/12/31	Title	
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				Size Document Number	
				LA-F251P	
Date: Tuesday, August 06, 2017				Rev	0.1
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Main Func = Other

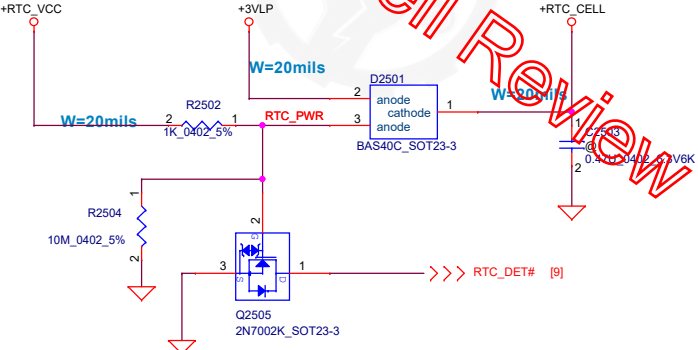
Screw hole/FD/EMI stop



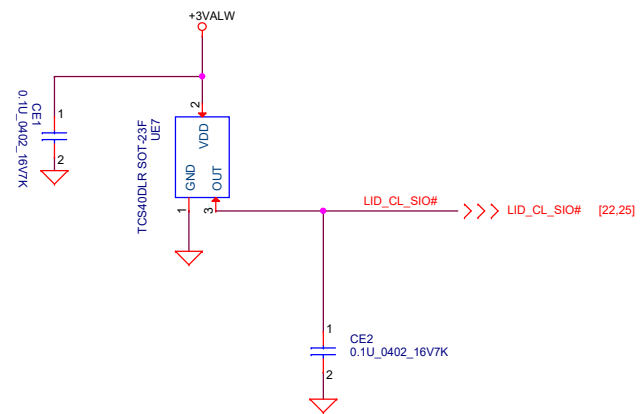
EMI reserve for PWR



Main Func = RTC

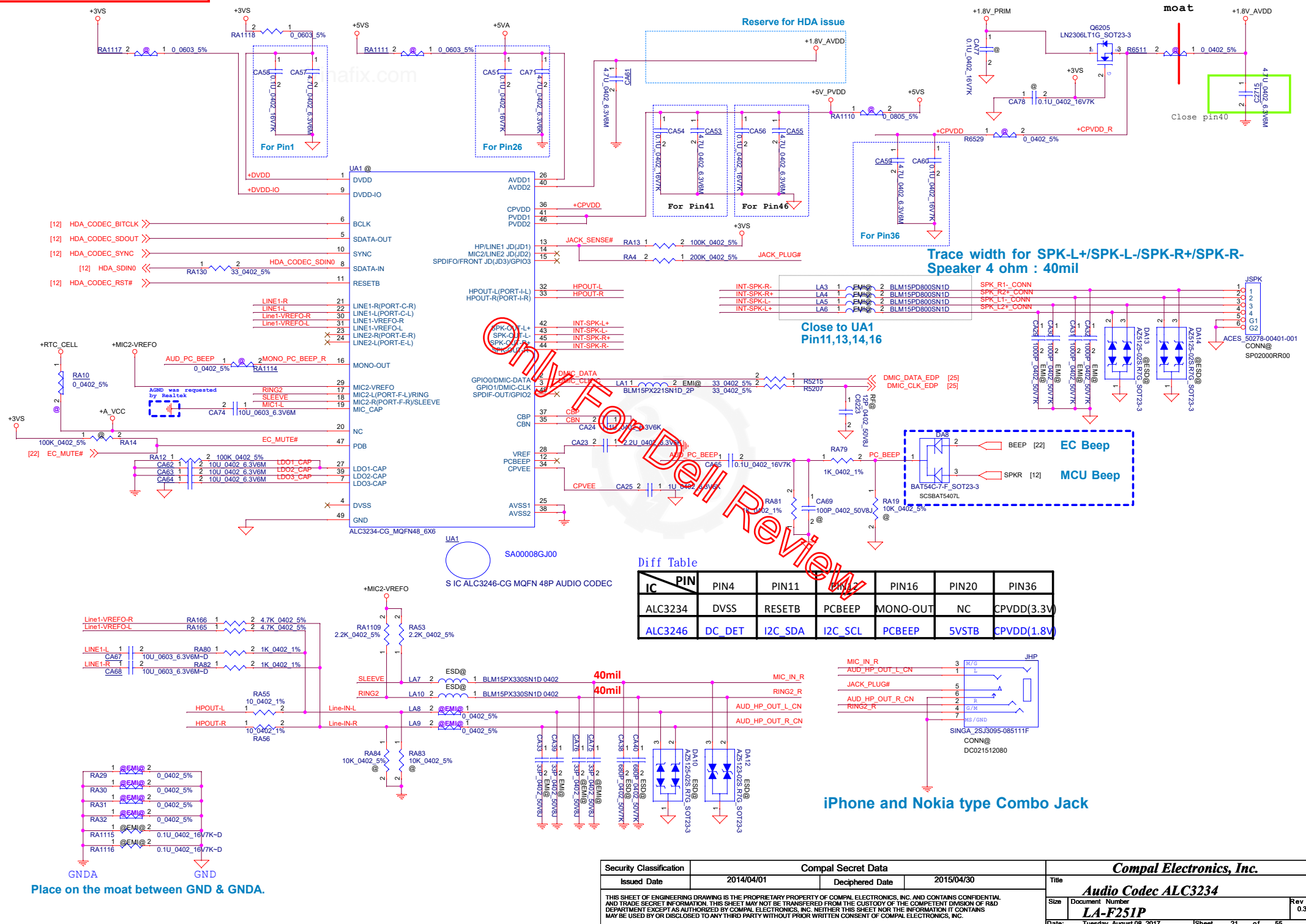


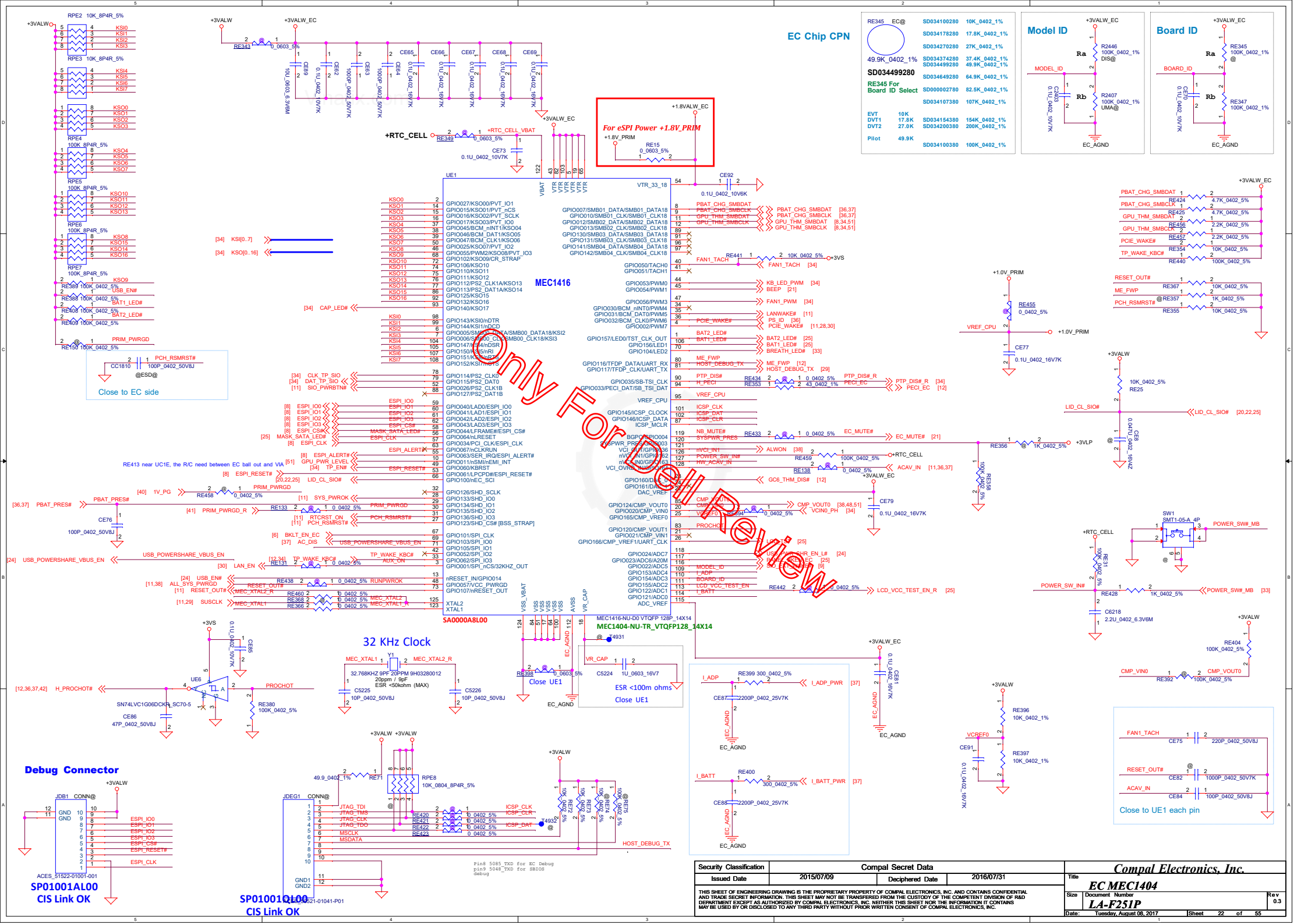
Main Func = LID Switch



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						Size		Document Number		Rev	
						LA-F251P		0.3			
						Date:		Tuesday, August 08, 2017		Sheet 20 of 55	

Main Func = Audio

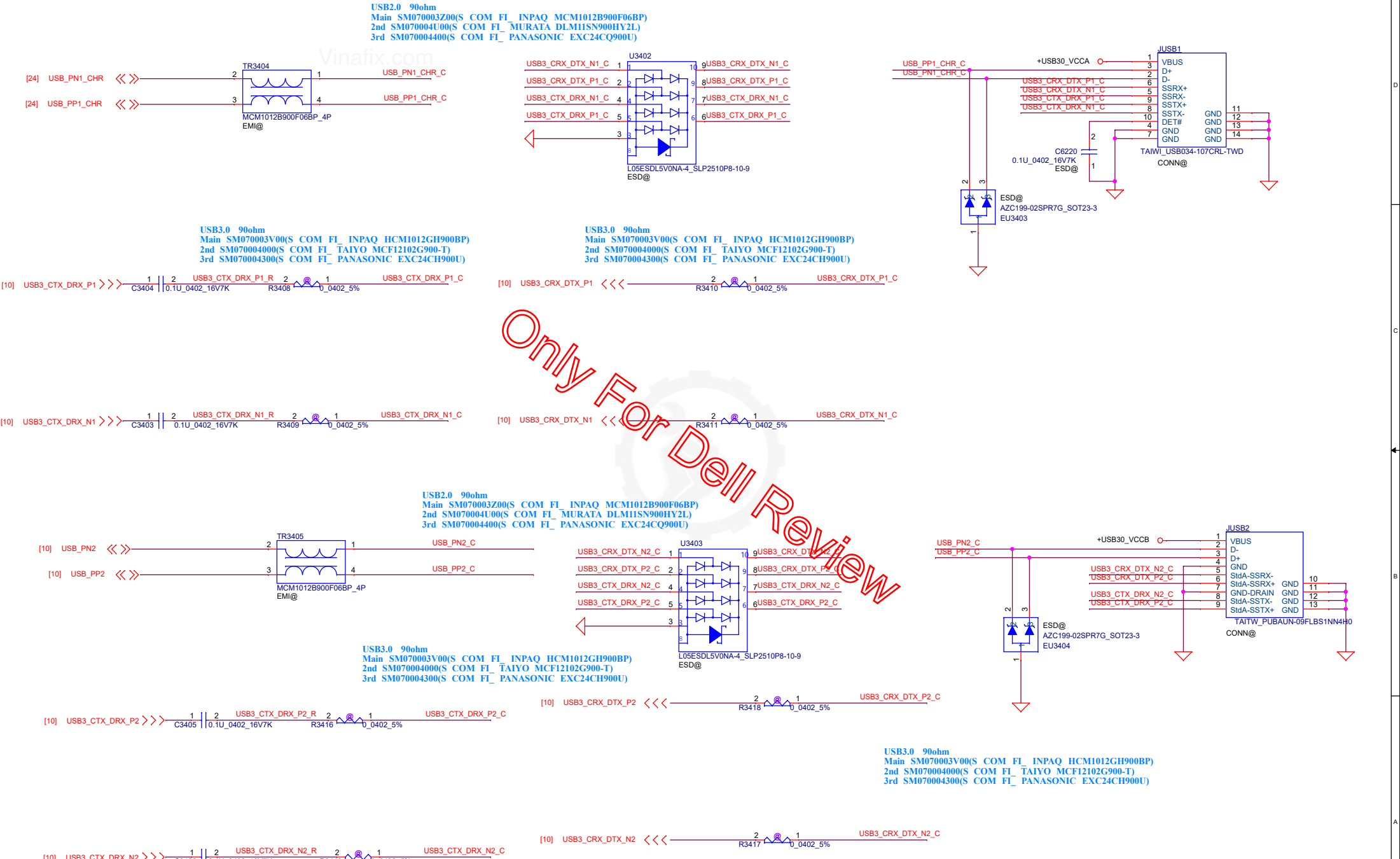




Main Func = USB3.0 Port1/Port2

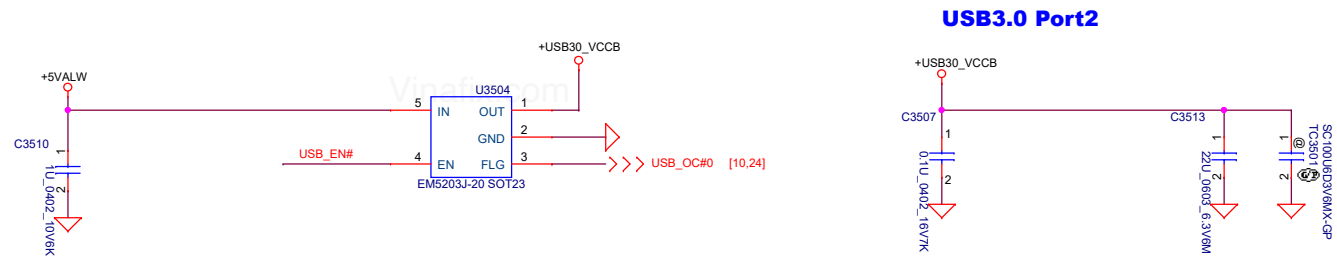
USB3.0 Port1

USB2.0 Port2 and USB2.0 Port3 are on IOBD



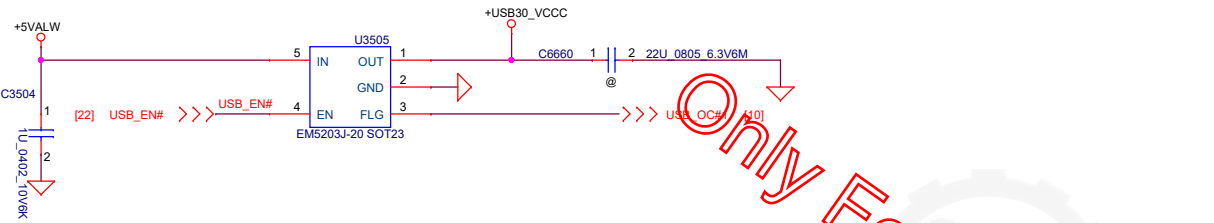
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Size		Document Number		Rev	
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Date:		Tuesday, August 08, 2017		Sheet 23 of 55	

Main Func = USB3.0 Port2

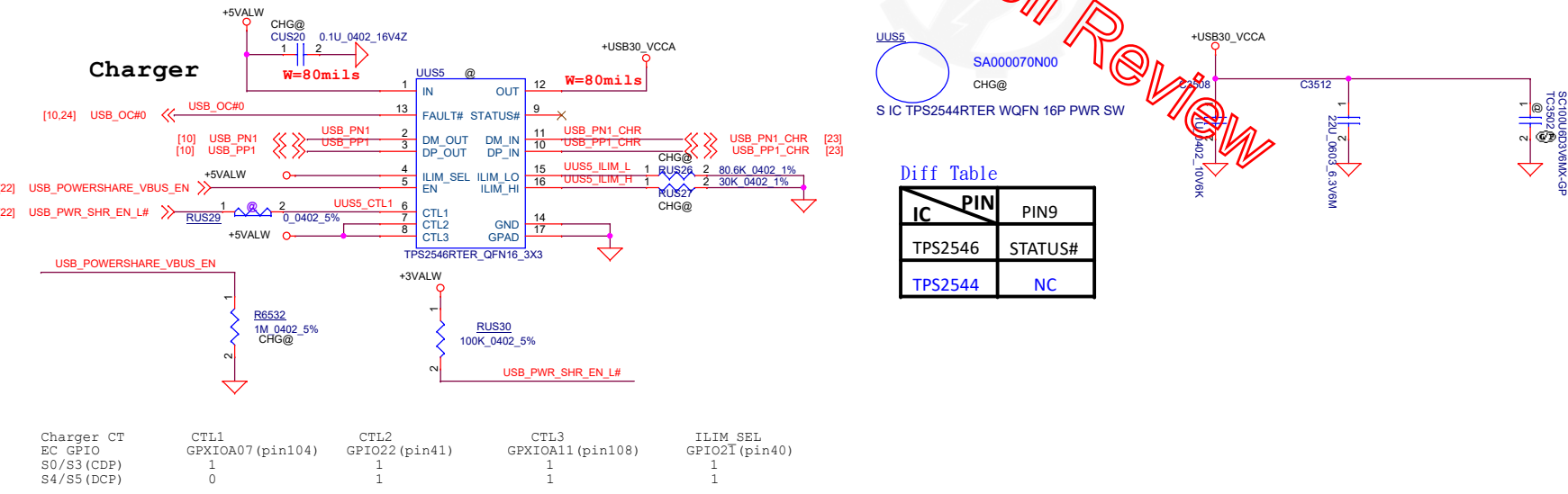


Main Func = USB3.0 Port3

USB3 Port3/USB2 Port1 (IO Board)



Main Func = USB Chager

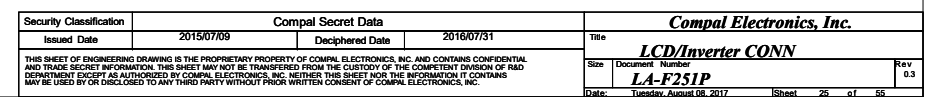
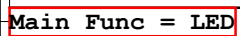


Diff Table

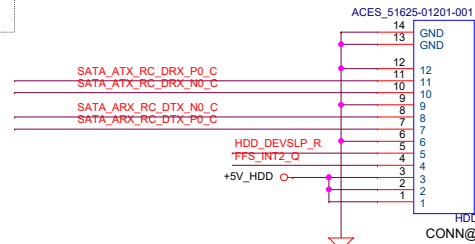
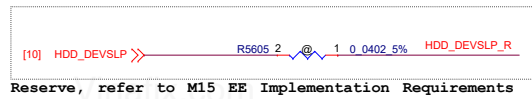
IC	PIN	PIN9
TPS2546	STATUS#	
TPS2544	NC	

Charger CT	CTL1	CTL2	CTL3	ILIM_SEL
EC GPIO	GPIOA07 (pin104)	GPIO22 (pin41)	GPIOA11 (pin108)	GPIO2I (pin40)
S0/S3 (CDP)	1	1	1	1
S4/S5 (DCP)	0	1	1	1

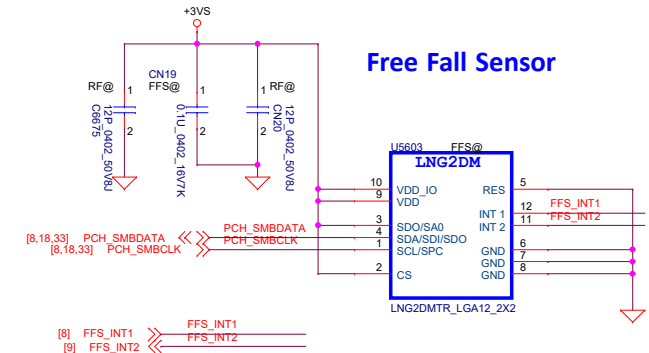
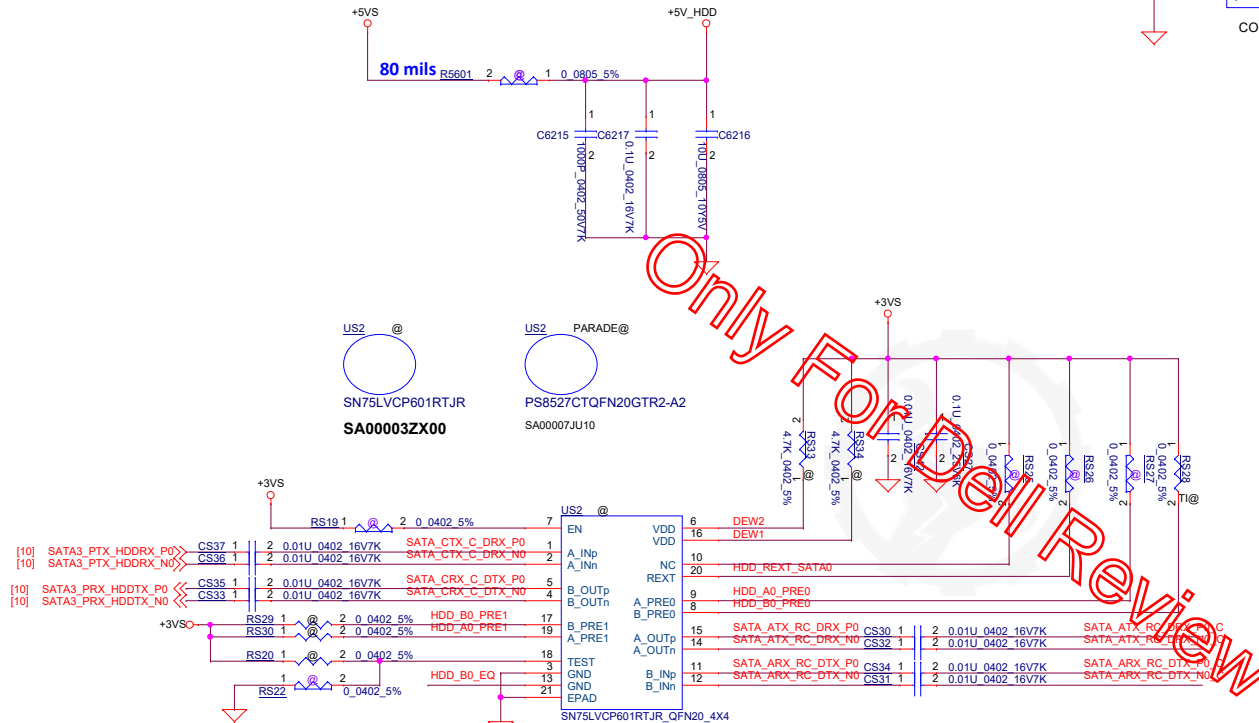
Main Func = CAM



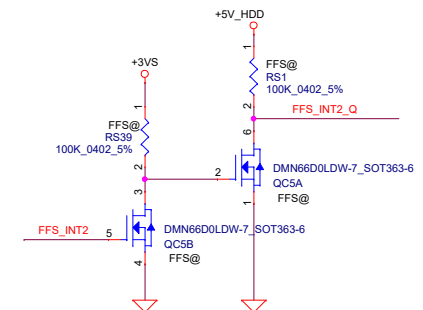
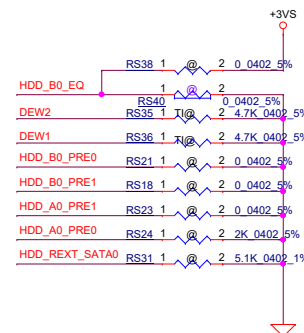
SATA HDD Connector



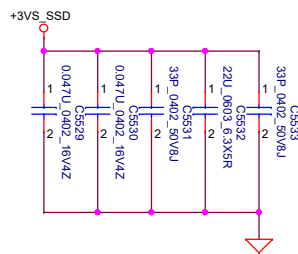
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	



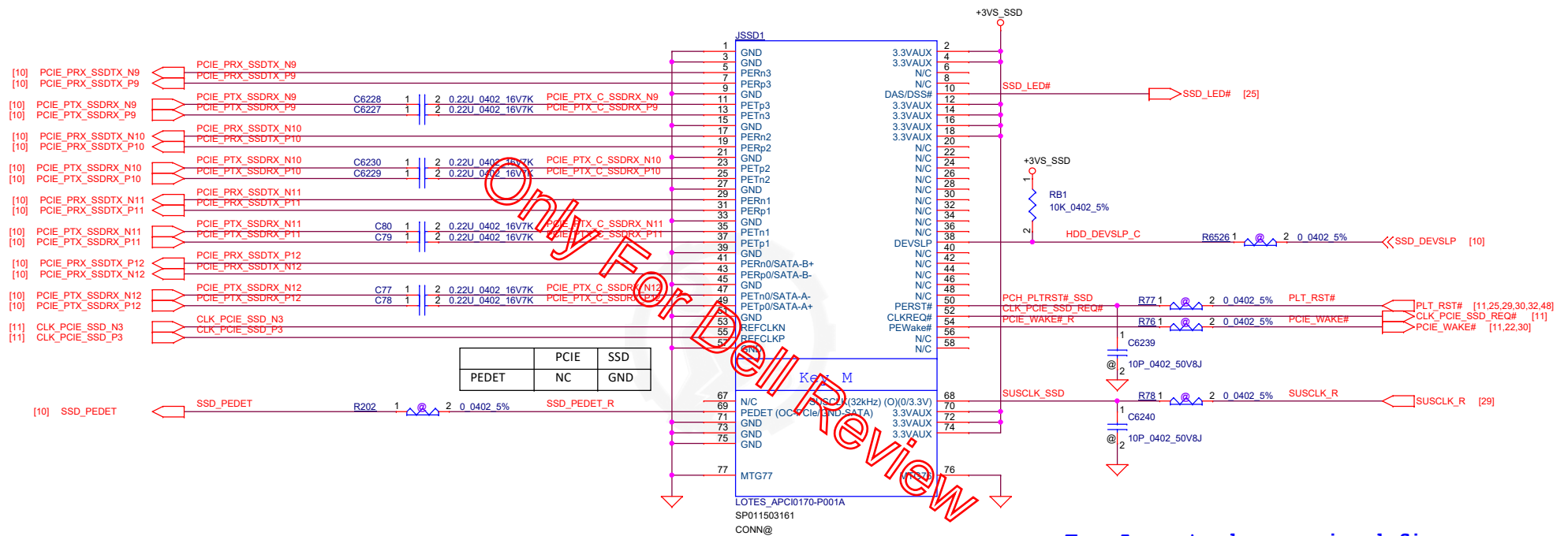
	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS28
TI	SA00003ZX00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA00007JU00	7.5K	NC	V	V	V	NC	NC



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				Size	Document Number	Rev
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SSD
NGFF Slot_2 Key M

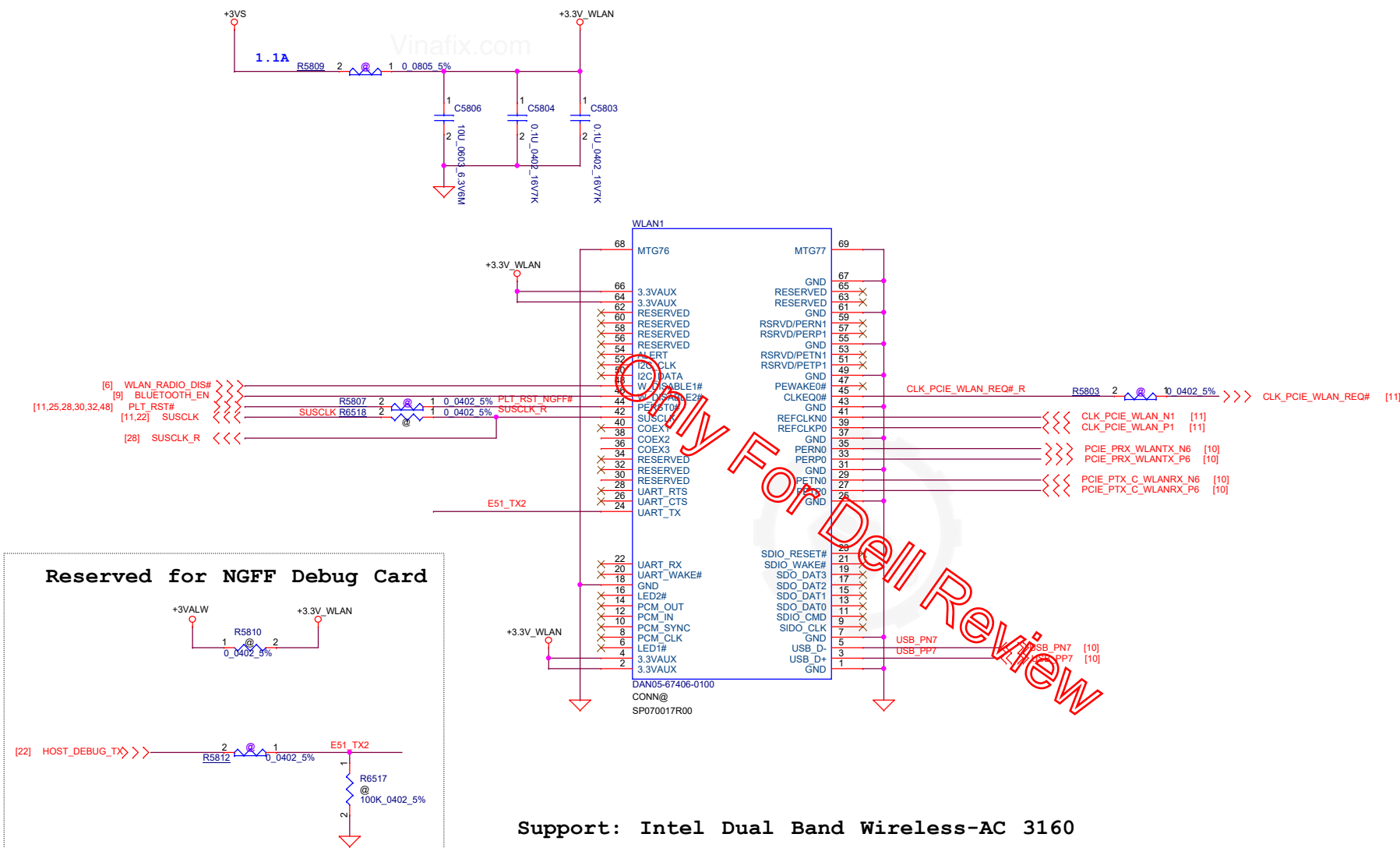


For Layout change pin define

44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C		

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				LA-F251P			0.3
				Date:	Tuesday, August 08 2017	Sheet	28 of 55

Main Func = WLAN

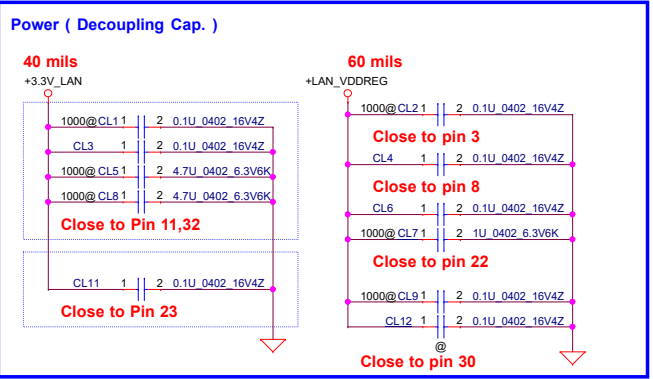
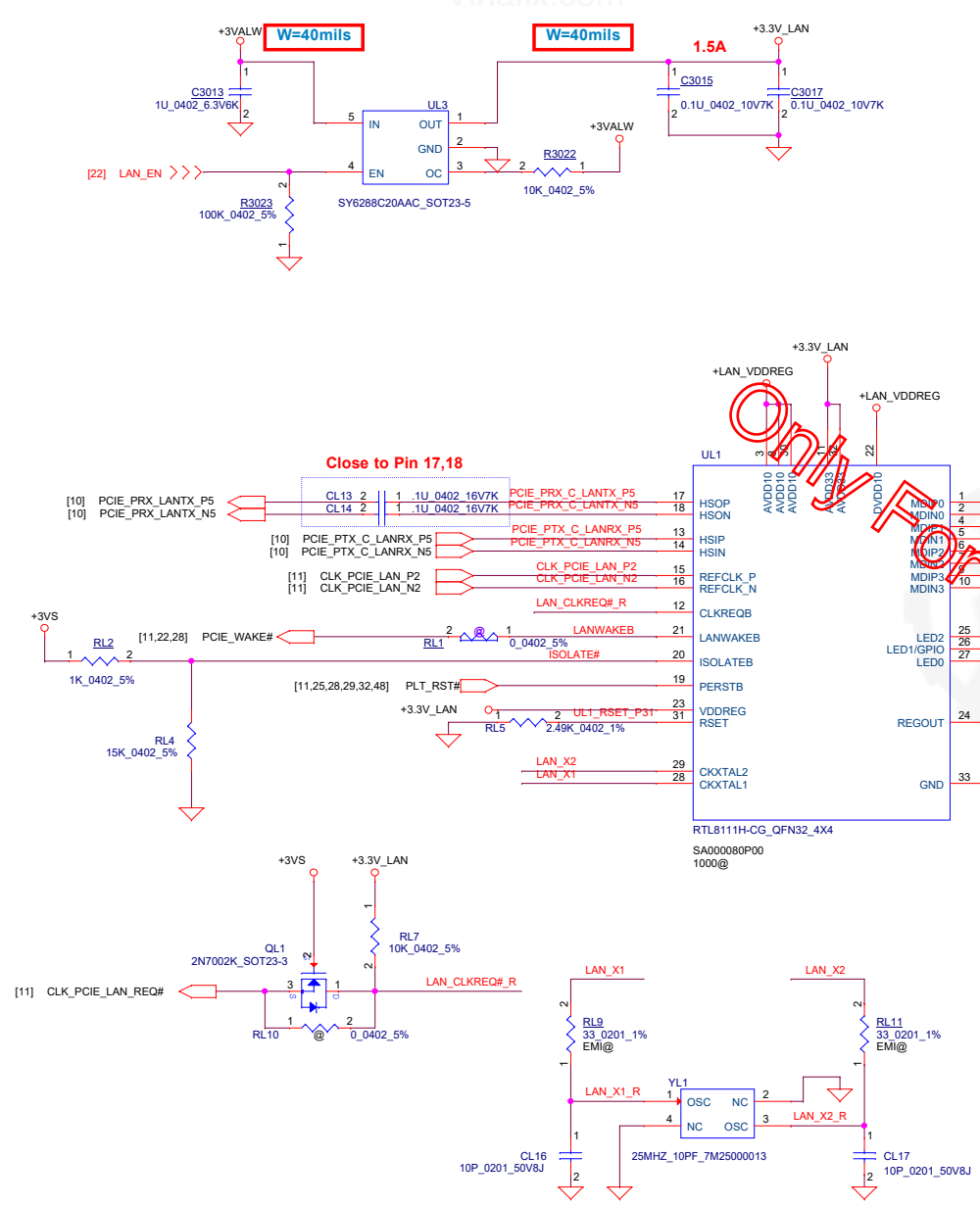


Support: Intel Dual Band Wireless-AC 3160

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Size		Document Number			Rev
		LA-F251P			0.3
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Main Func = LAN

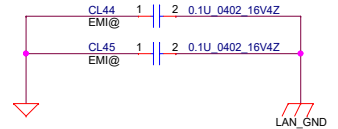
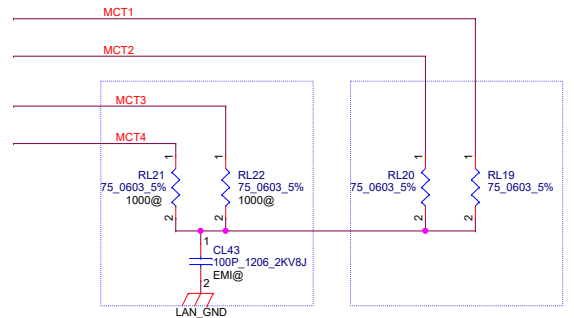
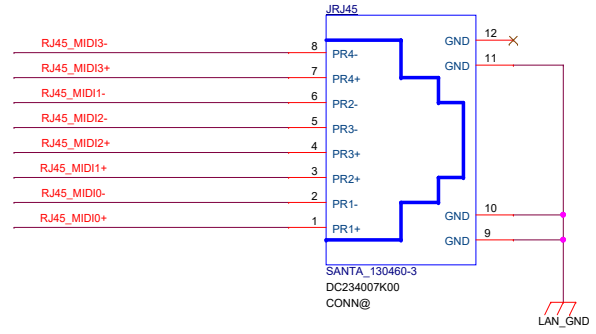
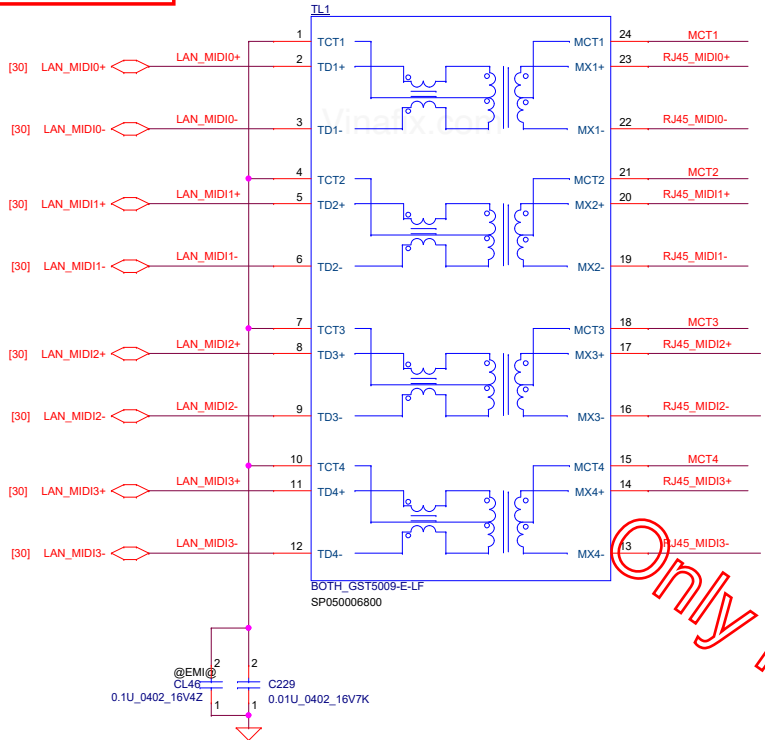
+3.3V_LAN rising time (10%~90%) need > 0.5ms and <100ms.



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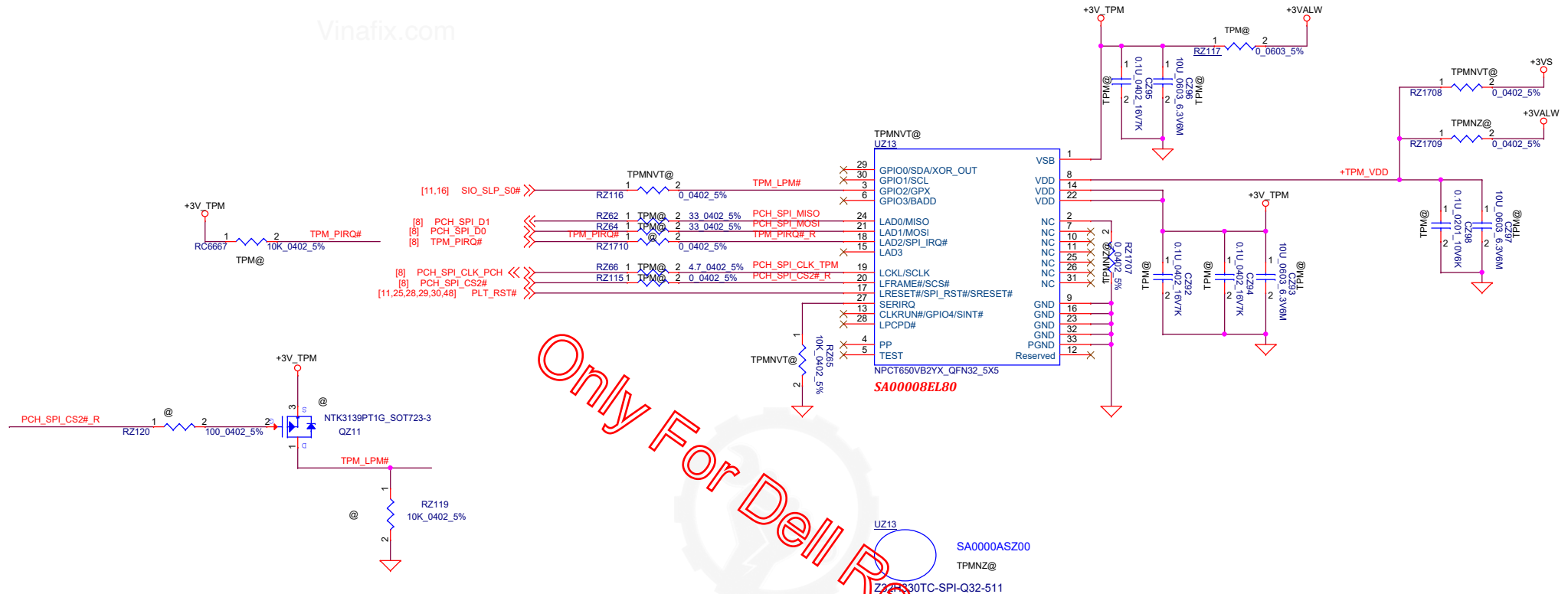
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Custom	LA-F251P
				Date:	Tuesday, August 08, 2017
				Sheet	30 of 55
				Rev	0.3

Main Func = LAN



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Size	Custom	Document Number	LA-F251P	Rev	0.3
Date:	Tuesday, August 08, 2017	Sheet	31	of	55

Main Func = TPM2.0

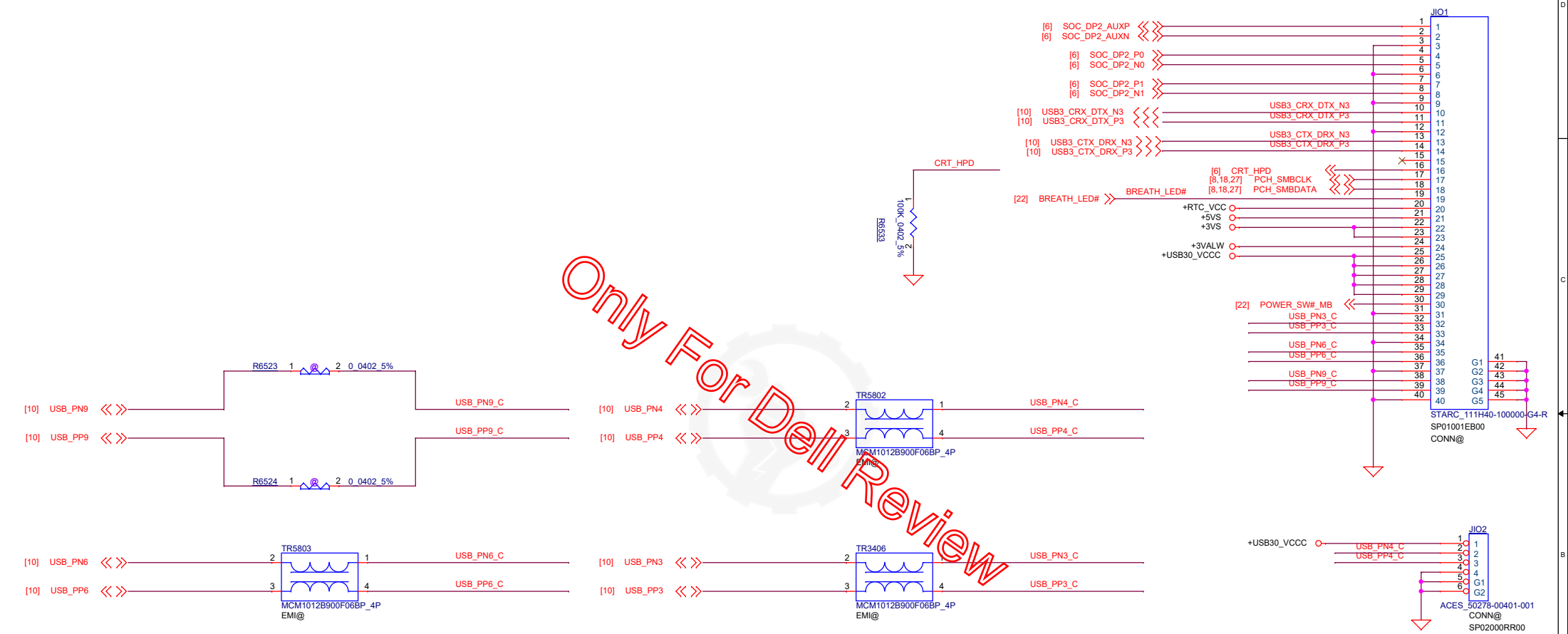


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						Size	Document Number		Rev 0.3
						Custom	LA-F251P		
						Date:	Sheet		32

Main Func = IO Connector

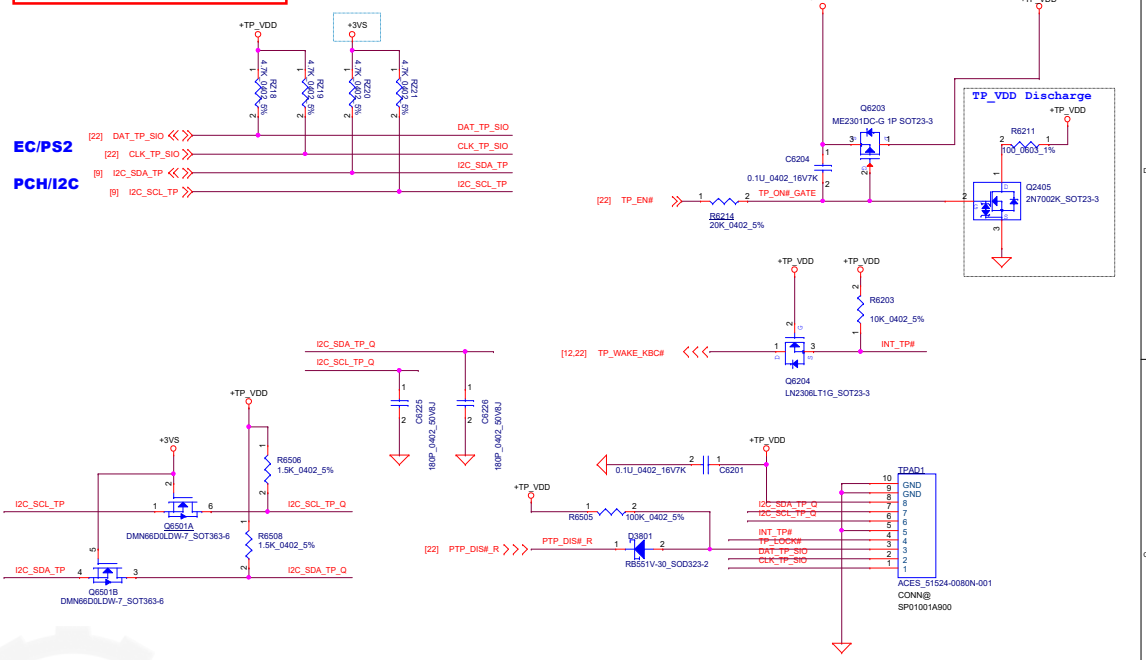
I/O Board Connector

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Size		Document Number		Rev	
		LA-F251P		0.3	
Date:		Tuesday, August 08, 2017		Sheet 33 of 55	

3	
	Main Func = TPAD



The image displays two main diagrams related to the TBM26 module's thermal management and sensor interface.

Top Diagram: PCB Layout and Sensor Interface

This diagram shows the physical layout of the TBM26 module, including the DIMM and CPU components. Key components and connections include:

- Thermal Sensor (THM26):** A 1-wire digital sensor connected to the CPU. The address is specified as X100_1100(4C), 1001_100X(98).
- Alert# Signal:** A 1-wire digital signal connected to the CPU. The signal is routed through a 10kΩ pull-up resistor (R2603) and a 10kΩ pull-down resistor (R2604).
- Thermal Sensor (THM26):** A 1-wire digital sensor connected to the CPU. The address is specified as X100_1100(4C), 1001_100X(98).
- Alert# Signal:** A 1-wire digital signal connected to the CPU. The signal is routed through a 10kΩ pull-up resistor (R2603) and a 10kΩ pull-down resistor (R2604).
- Thermal Sensor (THM26):** A 1-wire digital sensor connected to the CPU. The address is specified as X100_1100(4C), 1001_100X(98).
- Alert# Signal:** A 1-wire digital signal connected to the CPU. The signal is routed through a 10kΩ pull-up resistor (R2603) and a 10kΩ pull-down resistor (R2604).

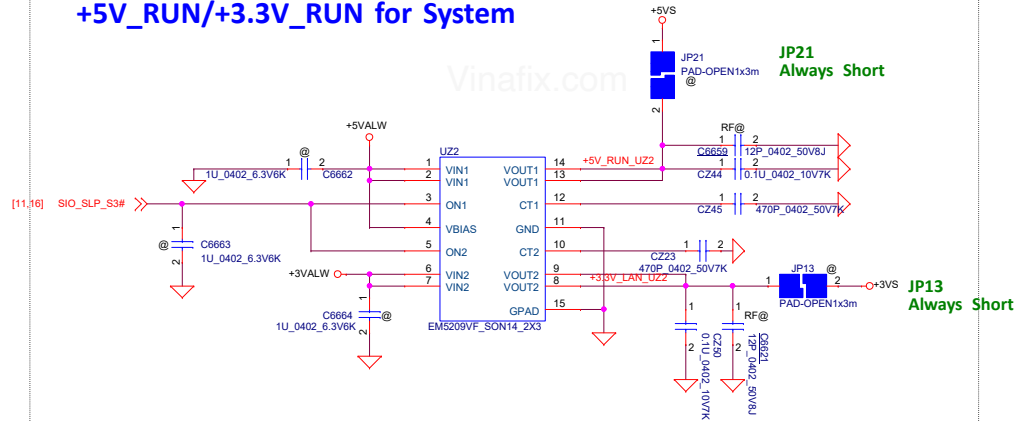
Bottom Diagram: Thermal Sensor Circuit

This diagram shows the electrical circuit for the thermal sensor, including the sensor itself and the associated components:

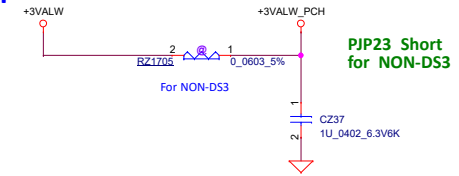
- Thermal Sensor (THM26):** A 1-wire digital sensor connected to the CPU. The address is specified as X100_1100(4C), 1001_100X(98).
- Alert# Signal:** A 1-wire digital signal connected to the CPU. The signal is routed through a 10kΩ pull-up resistor (R2603) and a 10kΩ pull-down resistor (R2604).
- Thermal Sensor (THM26):** A 1-wire digital sensor connected to the CPU. The address is specified as X100_1100(4C), 1001_100X(98).
- Alert# Signal:** A 1-wire digital signal connected to the CPU. The signal is routed through a 10kΩ pull-up resistor (R2603) and a 10kΩ pull-down resistor (R2604).
- Thermal Sensor (THM26):** A 1-wire digital sensor connected to the CPU. The address is specified as X100_1100(4C), 1001_100X(98).
- Alert# Signal:** A 1-wire digital signal connected to the CPU. The signal is routed through a 10kΩ pull-up resistor (R2603) and a 10kΩ pull-down resistor (R2604).

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

+5V_RUN/+3.3V_RUN for System



+3VALW_PCH for System



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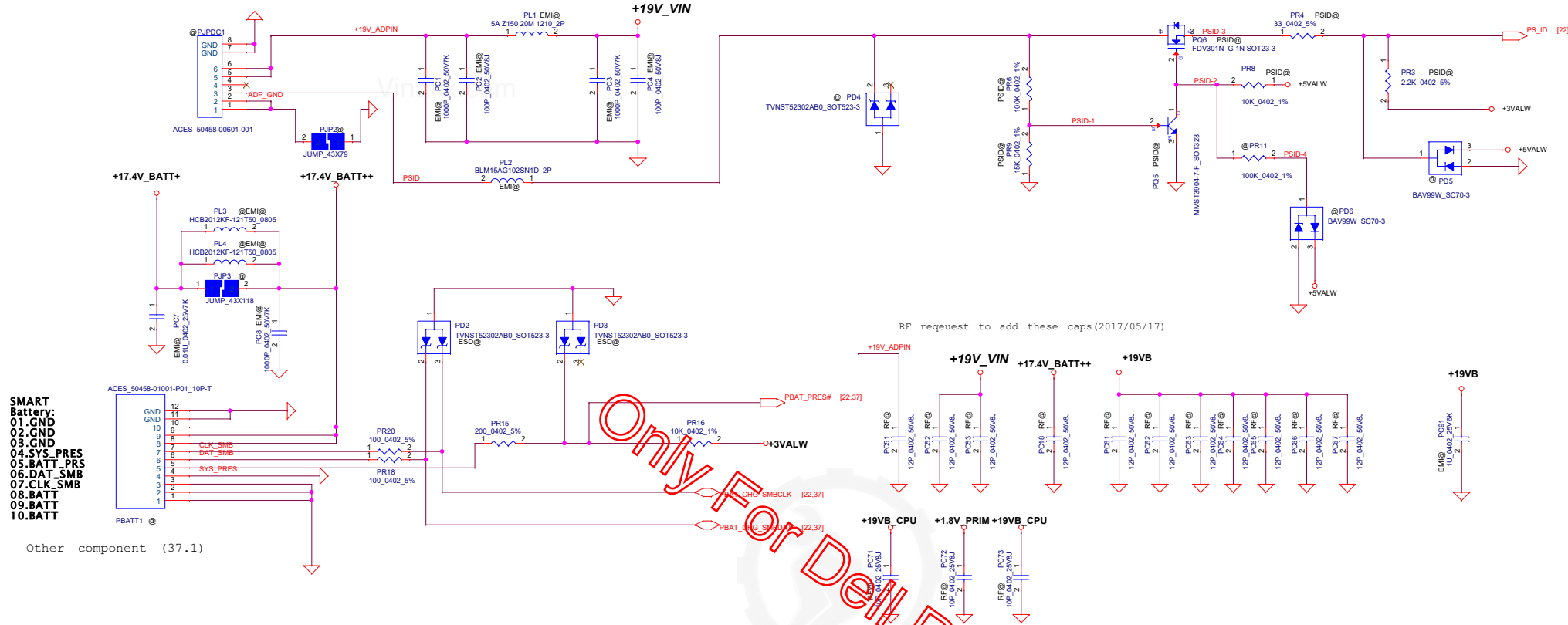
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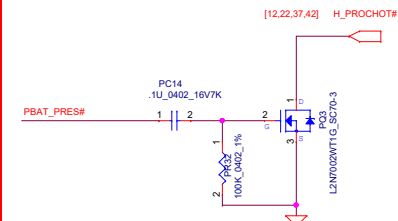


Title			
Power control			
Size	Document Number		Rev
	LA-F251P		0.3
Date:	Tuesday, August 08, 2017	Sheet 35 of 55	



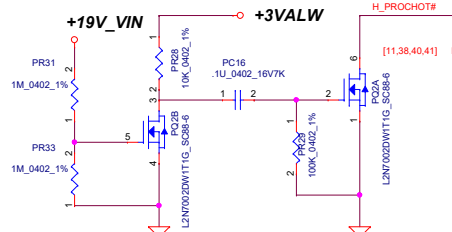
Adapter protection

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

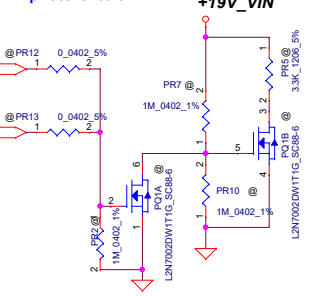


Battery protection

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW_PROCHOT# is issued by EC



Erp lot6 Circuit

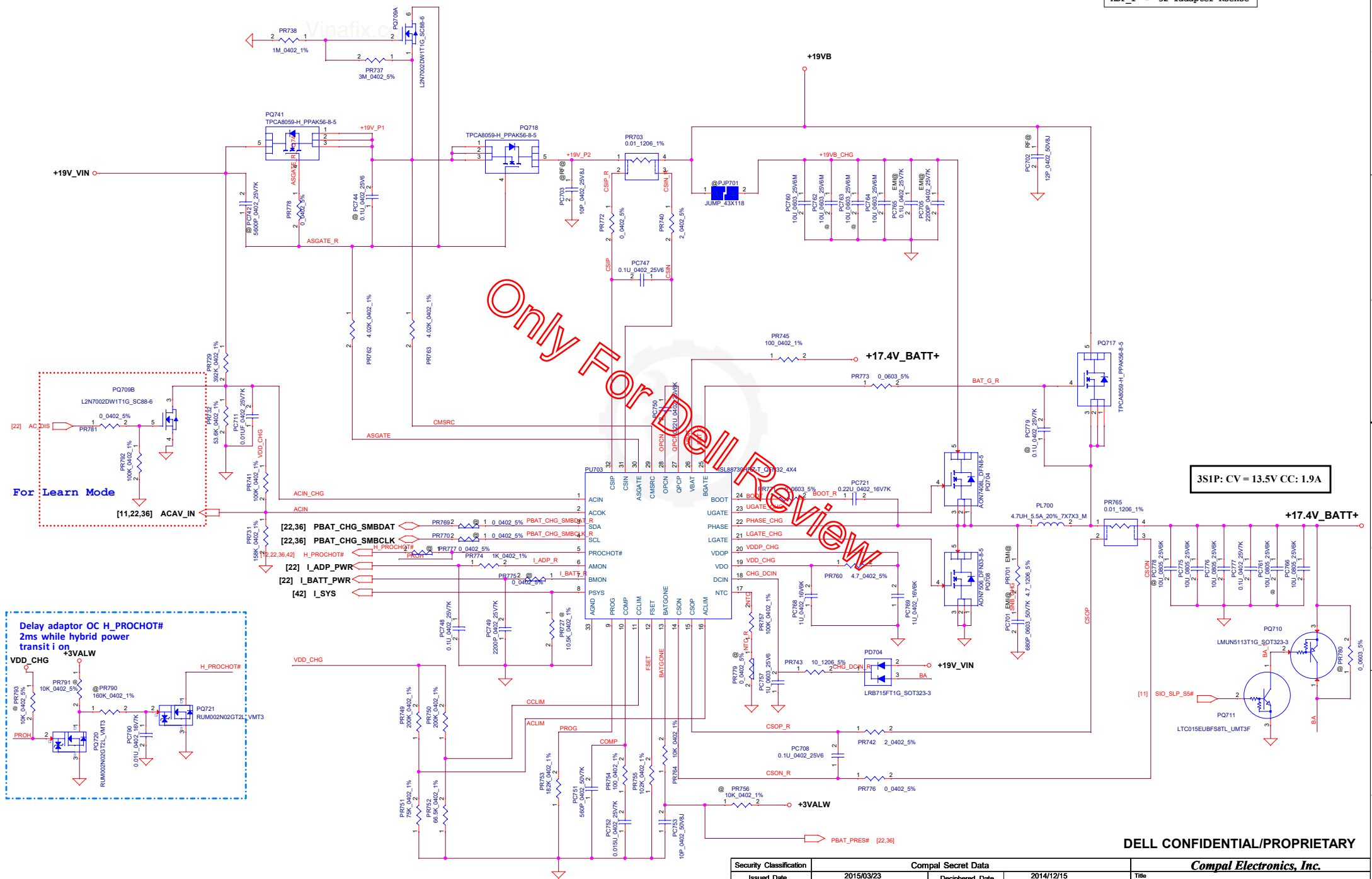


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Date:	Tuesday, August 08, 2017	Sheet	36 of 55	PWR DCIN/BATT CONN/OTP	

I_{ada}=0~2.30A (45W)

$$ADP_I = 32 \cdot I_{\text{adapter}} \cdot R_{\text{sense}}$$

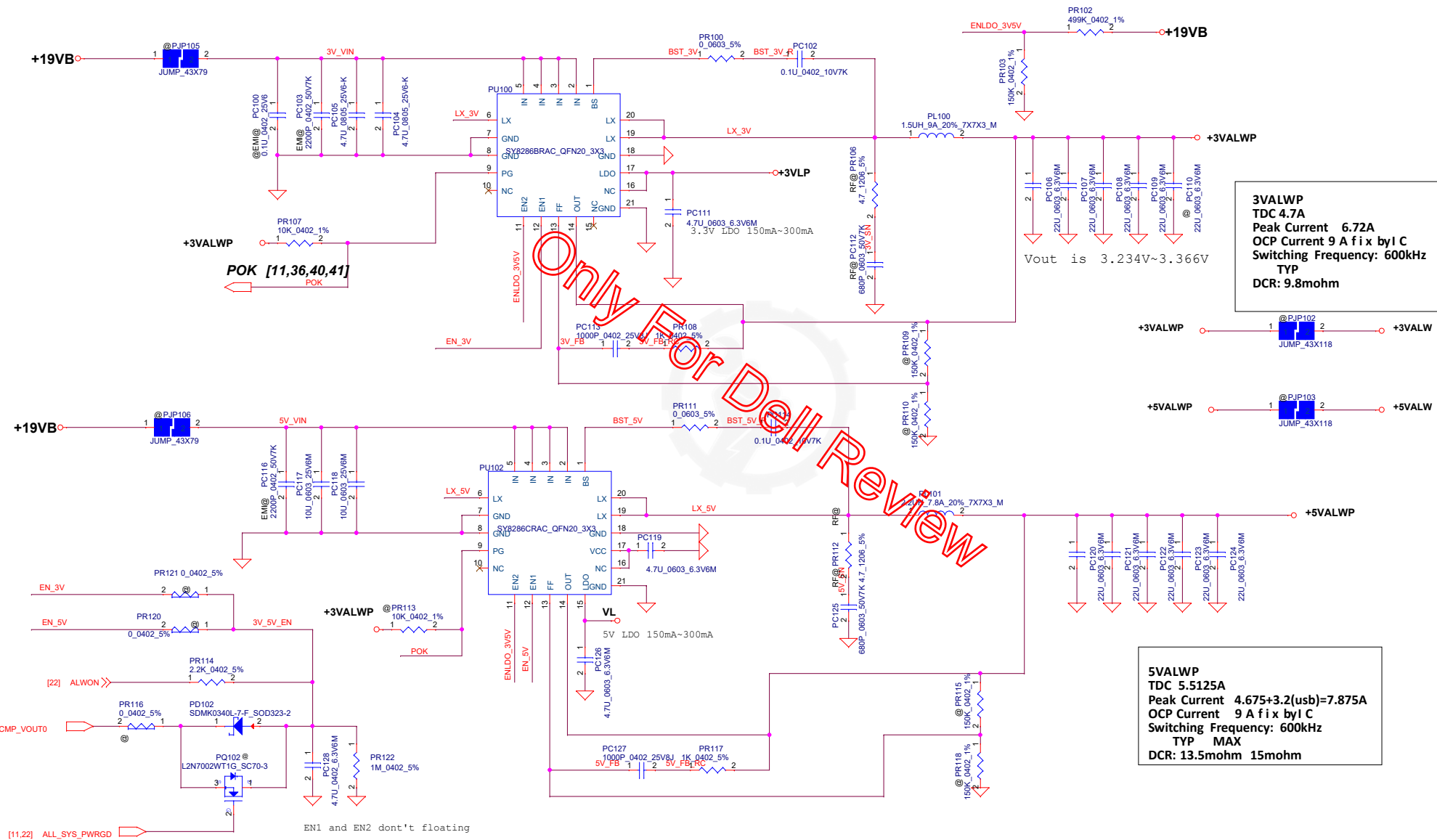


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			Docuement Number	Rev X010
Date: Tuesday, August 08, 2017			IShape: '9' x 16	

$3.3V \times 4.7A = 15.51W$
 $15.51 / 0.85 / 12 = 1.52A$
 $5V \times 5.5125A = 27.5625W$
 $27.5625 / 0.85 / 12 = 2.702A$

Vinafix.com



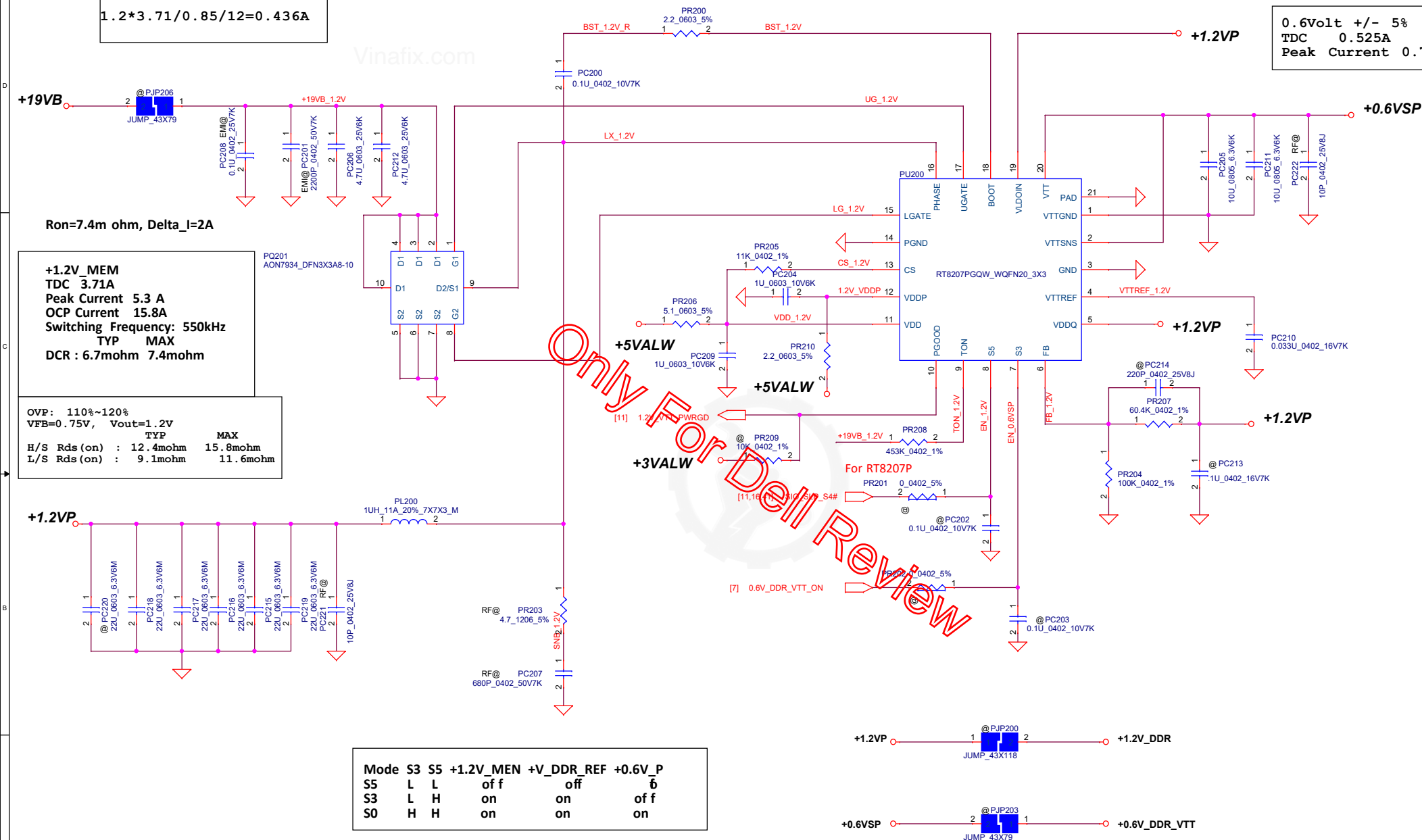
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Compal Electronics, Inc.			
Title			
PWR 3.3VALWP/5VALWP			
Size	Document Number	Rev	
		X01(0.2)	
Date:	Tuesday, August 08, 2017	Sheet	38 of 55

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$$1.2 \times 3.71 / 0.85 / 12 = 0.436 \text{ A}$$

0.6Volt +/- 5%
TDC 0.525A
Peak Current 0.75A



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Security Classification		Compal Secret Data			
Issued Date	2015/03/23	Deciphered Date	2014/12/15	Title PWR +1.2V_MEN/+0.6V_DDR_VTT	
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				Date:	Tuesday, August 08, 2017
				Sheet	39 of 55
				Rev	X01(0.2)

Input Current: 0.715A
 $1 \times 7.294 / 0.85 / 12 = 0.715A$

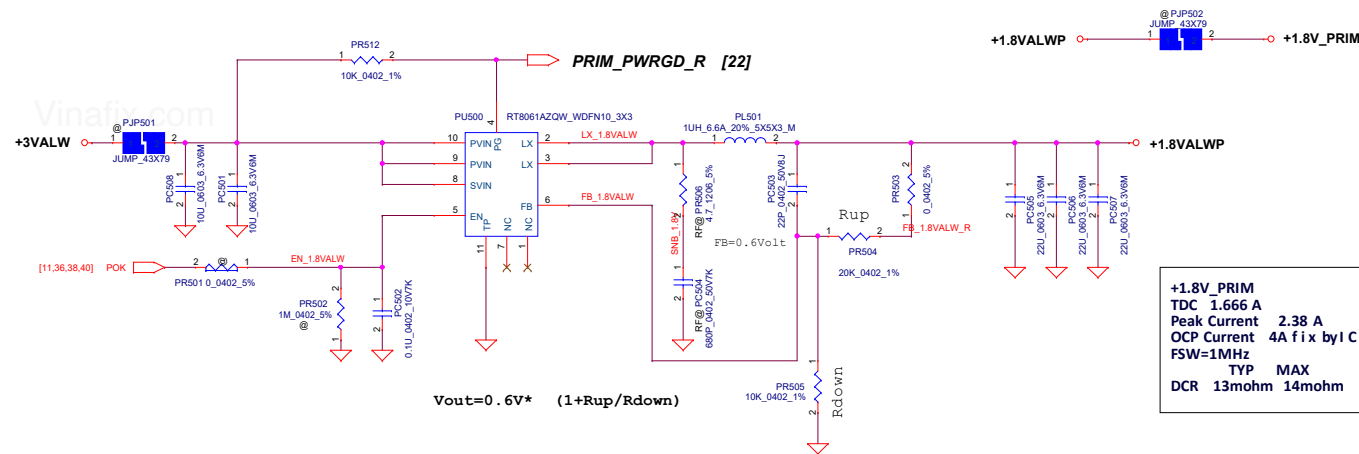
The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin3)
6A	Pull low
9A	Floating
12A	Pull high

+1.0V PRIM
TDC 7.294A
Peak Current 10.42 A
OCP Current 12 A Fix by IC
FSW=500KHz
TYP MAX
Choke DCR 6.2mohm , 7.2mohm

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Input Current: 1.176A
 $1.8 \times 1.666 / 0.85 / 3 = 1.176A$



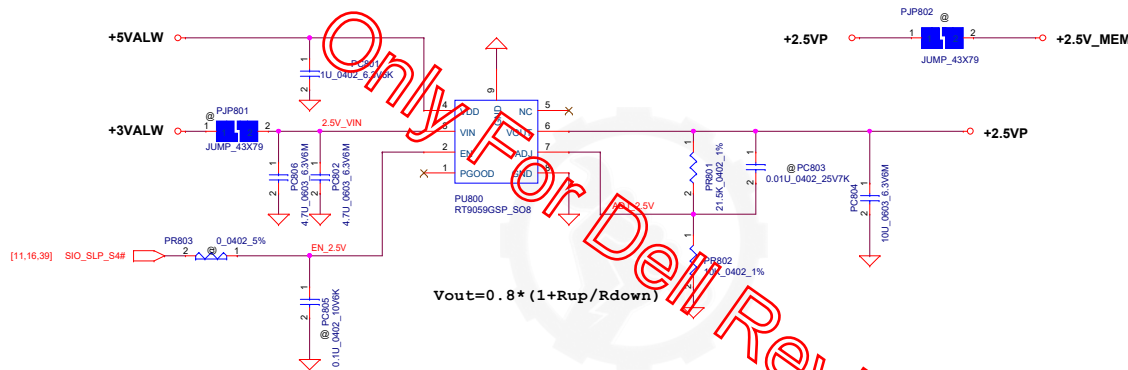
```

+1.8V PRIM
TDC 1.666 A
Peak Current 2.38 A
OCP Current 4A fix by I C
FSW=1MHz
      TYP    MAX
DCR 13mohm 14mohm

```

Input Current: 0.421A

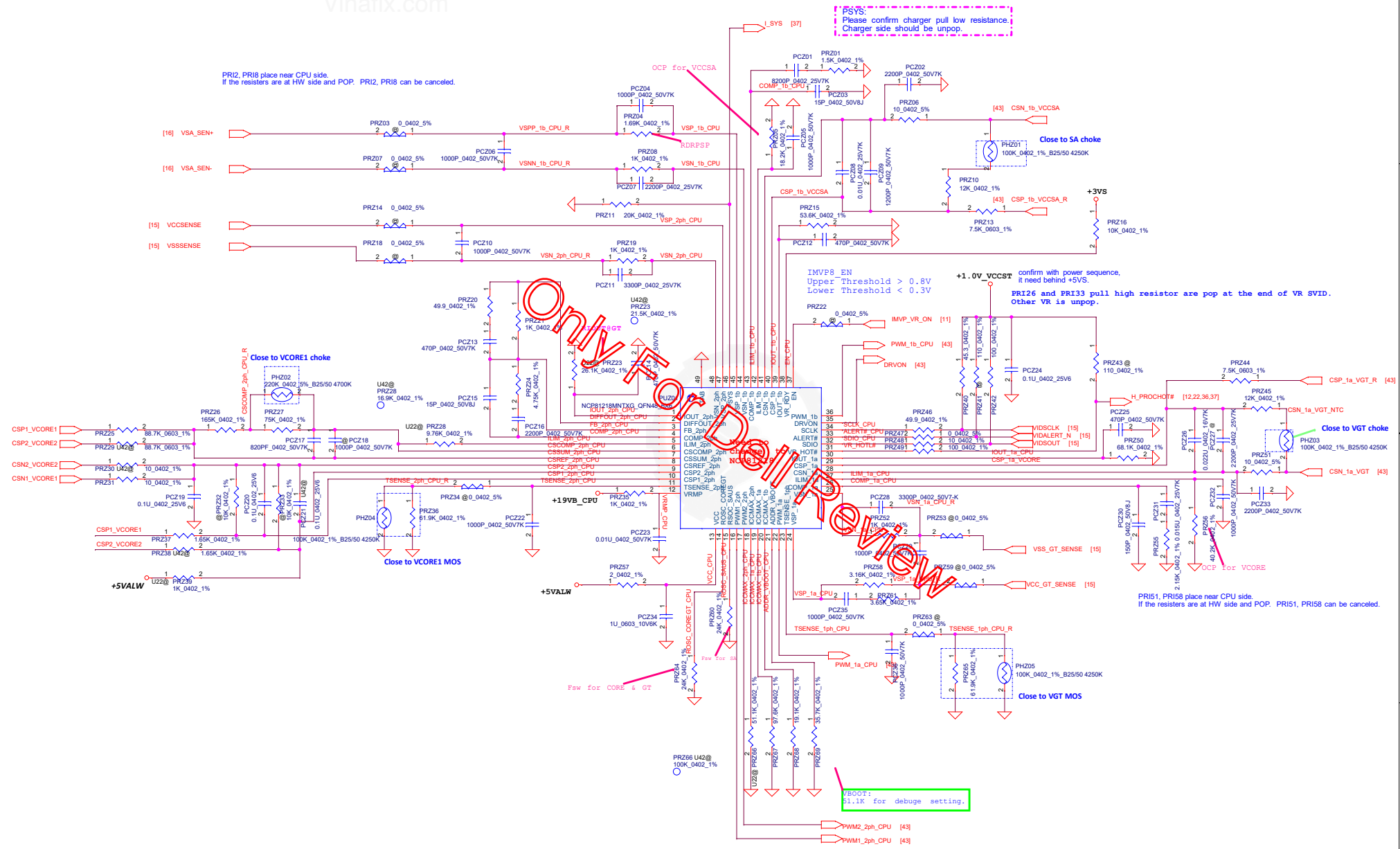
$2.5 \times 0.430 / 0.85 / 3 = 0.421A$



+2.5V
TDC 0.430 A
Peak Current 0.614 A
OCP Current 3.5A

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				C	
				Date:	Tuesday, August 08, 2017
				Sheet	41 of 55
					Rev X010(2)



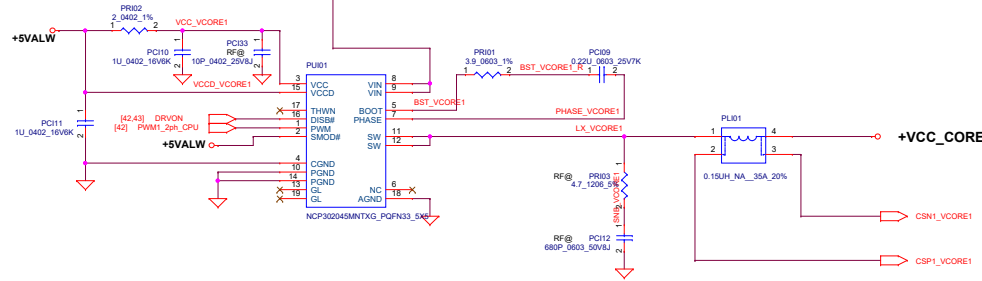
36.1&36.3

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								Size	Document Number
Date:		Tuesday, August 08, 2017				Sheet		42 of 65	

CPU POWER STAGES

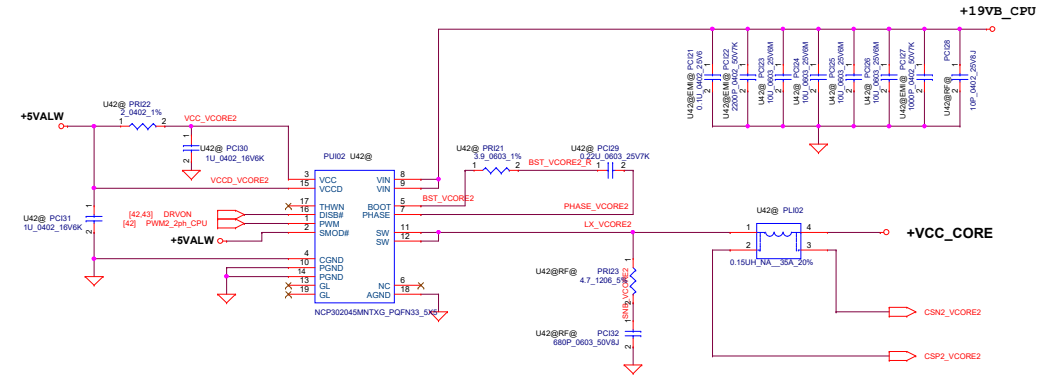
VCCIA
FSW=600kHz
TYP
H/S Rds(on) :11.7mohm ,
L/S Rds(on) :2.7mohm ,
MAX
14mohm
3.3mohm



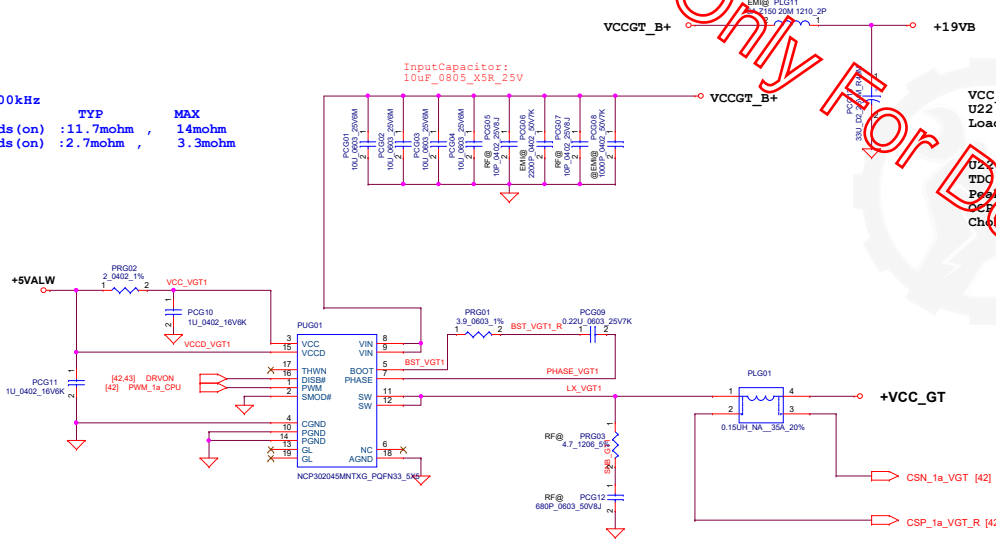
VCCIA
FSW=600kHz
TYP
H/S Rds(on) :11.7mohm ,
L/S Rds(on) :2.7mohm ,
MAX
14mohm
3.3mohm

VCC_core
U22 - 15W
Loadline : 2.4m-ohm

TDC 42A
Peak Current 64A
OCP current 70A
Choke DCR 0.9 +5% ohm (7*7*3)



VCCGT
FSW=600kHz
TYP
H/S Rds(on) :11.7mohm ,
L/S Rds(on) :2.7mohm ,
MAX
14mohm
3.3mohm

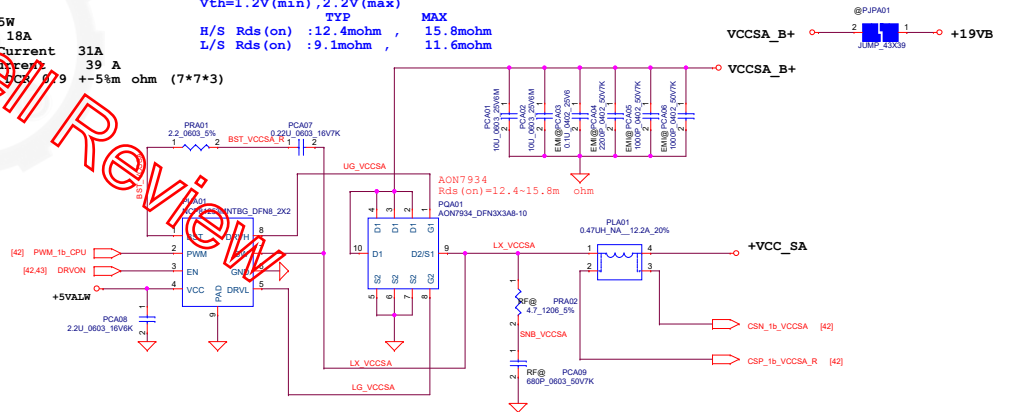


VCC_GT
U22 - 15W
Loadline : 3.1m-ohm
TDC 18A
Peak Current 31A
OCP current 39 A
Choke DCR 0.9 +5% ohm (7*7*3)

VCCSA
FSW=450kHz
Vin=20V
Vth=1.2V(min), 2.2V(max)
TYP
H/S Rds(on) :12.4mohm ,
L/S Rds(on) :9.1mohm ,
MAX
15.8mohm
11.6mohm

VCC_SA
Loadline : 10.3m-ohm

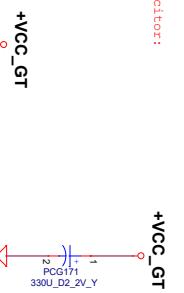
TDC 5A
Peak Current 6A
OCP current 12 A
Choke DCR 6.2 +5% ohm (5*5*3)



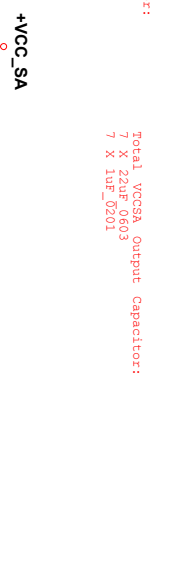
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2015/12/07	Deciphered Date	2017/01/31	Title	
				PWR CPUcore IA,GT and SA	
				Rev	X00
				Date	Tuesday, August 04, 2017
				Sheet	43 of 65



Total VCCORE Output Capacitor:
 3 X 330uF D1==>U22
 2 X 330uF D1==>U22
 28 X 22uF 0603==>U42
 20 X 22uF 0603==>U22
 26 X 1uF 0201==>U42
 35 X 1uF 0201==>U22

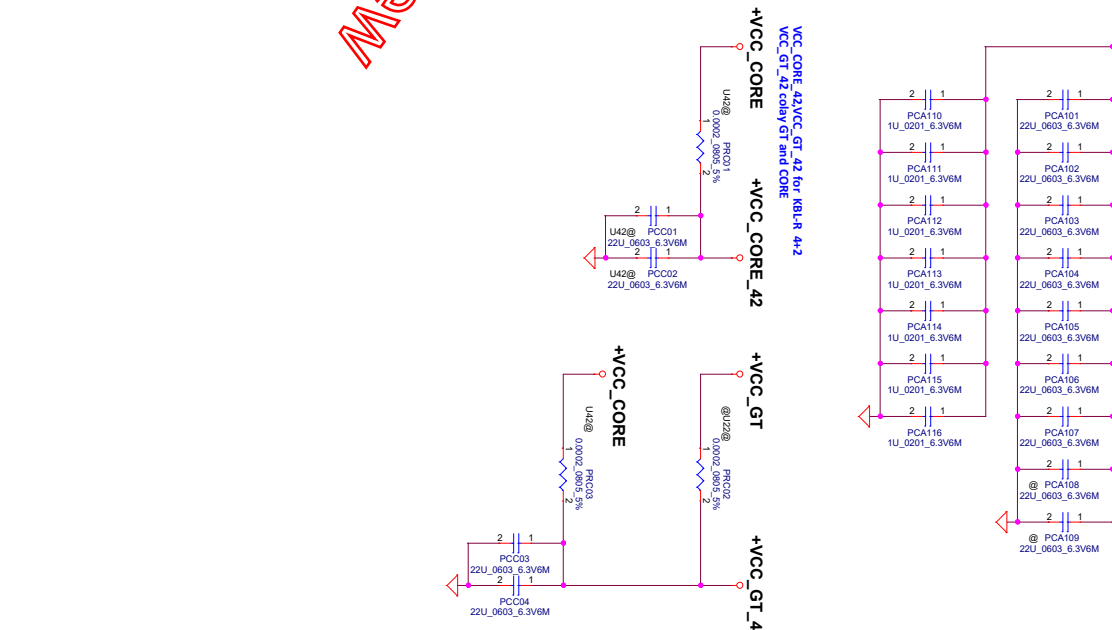
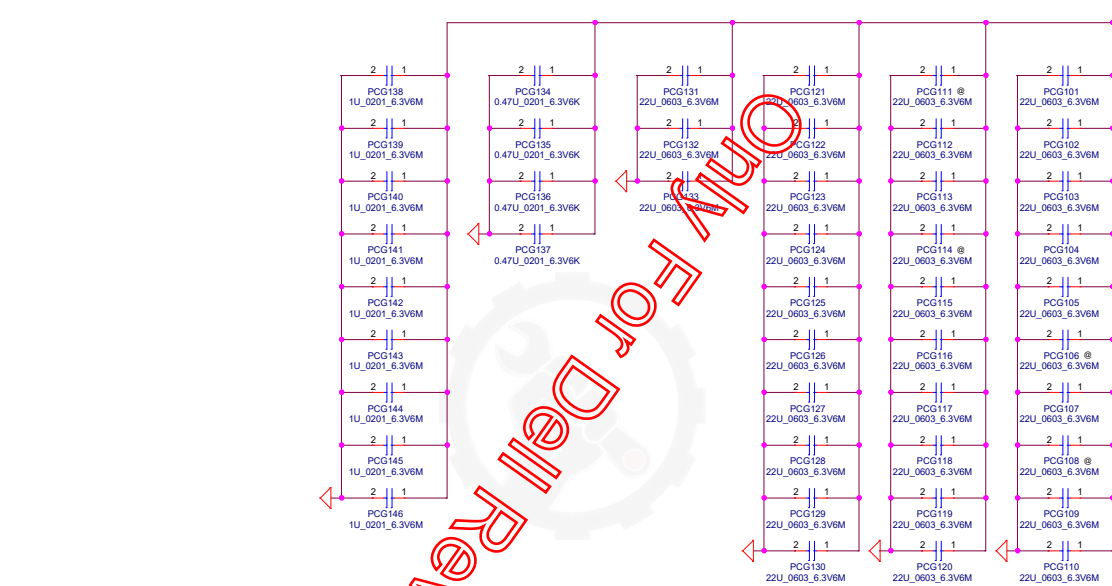
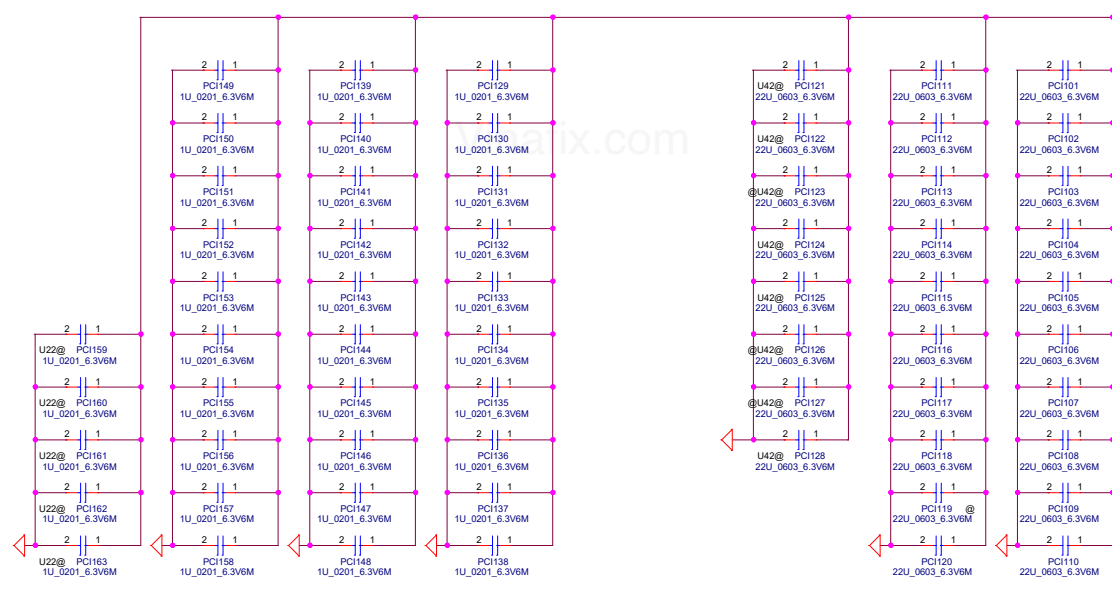


Total VCCGT Output Capacitor:
 1 X 330uF D1
 33X 22uF 0603 X5R
 4X0.47uF 0201
 9X 1uF 0201



Total VCCSA Output Capacitor:
 7 X 330uF D1
 7 X 22uF 0603
 4X0.47uF 0201
 7 X 1uF 0201

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				Title	
				PWR_CPU&VGA & SA MISC	
Drawn	Document Number			Issue	Rev
					200
Date	Thursday, August 08, 2017	Issue	44	of	63

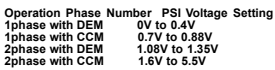
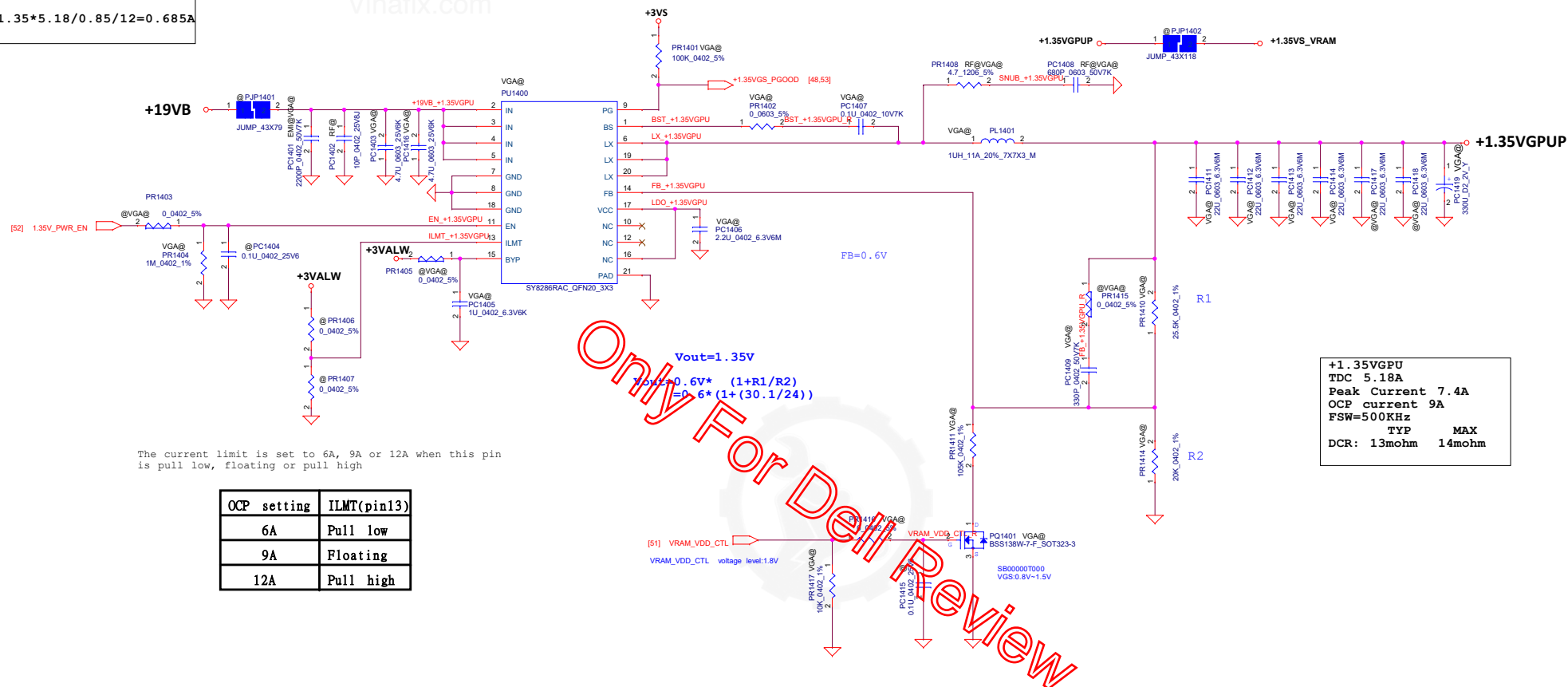


Figure 10: Schematic diagram of the proposed 16-to-1 multiplexer. The diagram shows a hierarchical structure of 2-to-1 multiplexers. At the top, there are four 2-to-1 multiplexers labeled VOAG_P12102, VOAG_P12103, VOAG_P12104, and VOAG_P12105, each with inputs 2 and 1. These are connected to four intermediate 2-to-1 multiplexers labeled VOAG_P12106, VOAG_P12107, VOAG_P12108, and VOAG_P12109. These intermediate multiplexers are then connected to a final 2-to-1 multiplexer at the bottom labeled VOAG_P12110, which has inputs 2 and 1. The output of the final multiplexer is labeled 11_0002_0900K.

+GPU CORE	
TDC=29.7A	
Peak Current 59.2A	
OCP=	
DCR:0.98mohm +-5%	
	MAX
H/SRds(on):	6.7mohm 8.5mohm
L/SRds(on):	4.7mohm 5.9mohm

Input Current: 0.685A
 $1.35 \times 5.18 / 0.85 / 12 = 0.685A$

Vinafix.com



The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

OCP setting	ILMT(pin13)
6A	Pull low
9A	Floating
12A	Pull high

+1.35VGPU
TDC 5.18A
Peak Current 7.4A
OCP current 9A
FSW=500KHz
TYP MAX
DCR: 13mohm 14mohm

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				Date:	Tuesday, August 08, 2017
				Sheet	46 of 55

Version Change List (P. I. R. List)

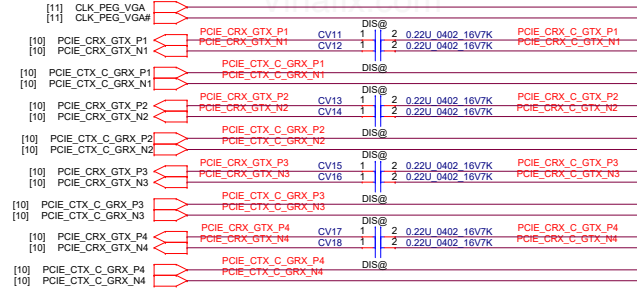
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	PWR	5/4/2017	COMPAL	For charger setting.	1 change PR1418 to PR792 2 change 10K to 100 K ohm	EVT->DVT1
2	37	PWR	5/4/2017	COMPAL	to reservie PR793 to fine tune the delay time	Add PR793 for 10k ohm at @	
3	46	PWR	5/4/2017	COMPAL	For VRAM output setting	@ PC1417,PC1418 for 22uF and @PC1419 for 330uF	
4	44	PWR	5/4/2017	COMPAL	For VCC_CORE_42,VCC_GT_42 for KBL-R 4+2 VCC_GT_42 co lay GT and CORE setting.	Add PRC04,PRC05,PRC06 for SOLDER_PREFORMS.	
5	36	PWR	5/4/2017	COMPAL	For DCIN_PSID setting.	Change PQ5 from SB00000Z500 to SB00000Z2R00.	
6	43	PWR	5/4/2017	COMPAL	change location name	Change location name fromPHI11 to PLI11.	
7	37	PWR	5/9/2017	COMPAL	For charger setting.	Change PQ1,PQ2,PQ709 from SB00000PV00 to SB00000DH00.	
8	36	PWR	5/9/2017	COMPAL	for adaptor to delay proshot 2ms setting	change PR791 to @	
9	42	PWR	5/9/2017	COMPAL	To avoid leakage proble to change power source to +5VALW	to connecto PRZ39,PRZ57 to +5VALW	
10	43	PWR	5/9/2017	COMPAL	To avoid leakage proble to change power source to +5VALW	to connecto PRI02,PRI22,PRG02,PCA08 to +5VALW	
11	36	PWR	5/9/2017	COMPAL	to add 12p cap by RF request	to add PC18 (12pF)	
12	36	PWR	5/17/2017	COMPAL	to add 12p cap by RF request	to add 10 cap for PC51,PC52,PC53,PC61,PC62,PC63,PC64,PC65,PC66,PC67	
13	43	PWR	5/17/2017	COMPAL	change to 12p and change to RF@	to add 12p cap for PCI05	
14	42	PWR	5/17/2017	COMPAL	according to test result to change these component	change PRZ25,PRZ29 to 88.7K change PRZ21 to 1K change PRZ23 to 21.5K change PRZ04 to 1.69K change PRZ15 to 53.6K change PRZ50 to 68.1K change PRZ58 to 2.16K change PRZ55 to 2.15K change PCZ27 to 2.2K change PCZ31 to 2200p	
15	44	PWR	5/17/2017	COMPAL	according to test result to change these component	PCG111,PCG106,PCG144,PCG108 change to @ PCI172 remove	
16	36,43,38,40	PWR	6/26/2017	COMPAL	RF request to add these caps and RC 5V,1V Snubber RC	to add 10pF for PC71,PC72,PR73, PCI33,PCI28,PCG07,PCG05 to ad PR112,PC125,PR307,PC308 in BOM	DVT1->DVT2
17	37,38,39,40,41,42,43,45,46	PWR	6/26/2017	COMPAL	to reduce component	PR773,PR769,PR770,PR777,PR775,PR739,PR120,PR121,PR116,PR201,PR202, PR301,PR304,PR311,PR303,PR501,PR803, PRZ22,PRZ03,PRZ07,PRZ14,PRZ18,PRZ34,PRZ53,PRZ59,PRZ68,PR104,PR1106,PR1116,PR1117,PR1115,PR1403,PR1405,PR1415	
18	46	PWR	6/26/2017	COMPAL	to reduce 1.35V ripple	to add PC1419 in BOM	
19	36	PWR	6/26/2017	COMPAL	EMI request to add this bead in BOM	to add PL1 in BOM	
20	38,45	PWR	6/26/2017	COMPAL	Common part design change package	change 0603 to 0402 (PC128,PC1101) change 0805 to 0603 (PC106,PC107,PC108,PC109,PC110,PC1146)	
21	36	PWR	6/27/2017	COMPAL	RF issue	change netname to +19VB_CPU	
22	43	PWR	6/27/2017	COMPAL	material shortage issue	BOM option to add PCI13,remove PCI14	
23	43	PWR	6/28/2017	COMPAL	EMI request to add RC snubber in BOM	to add PR701(4.7 ohm),PC701(680p) in BOM	
24	42	PWR	7/7/2017	COMPAL	GT_CORE OVP	to change PCZ30 to 150p and PCZ31 to 15n	
25	44	PWR	7/25/2017	COMPAL	to remove co-lay footprint	to remove PRC04,PRC05,PRC06	DVT2->Pilot
26	36	PWR	7/31/2017	COMPAL	EMI request to add 1uF in the +19VB to GND	to add PC91	
27	39	PWR	7/31/2017	COMPAL	RF request to add two for +0.6VSP and +1.2VP	to add PC221,PC222	
28	36,37,38,43,45	PWR	7/31/2017	COMPAL	to remove co-lay footprint	to remove PJF1,PL5,PL704, PL102,PL103,PCI14,PJPG01,PJPI01,PL1101	
29	45	PWR	7/31/2017	COMPAL	to remove co-lay footprint	to remove PC1154	
30	40	PWR	8/7/2017	COMPAL	EMI request to mount PC302	to change PC302 to EMI@	
31	43	PWR	8/7/2017	COMPAL	EMI request to mount the VCCSA input cap	to change PCA03,PCA04,PCA05,PCA06 to EMI@	
32	39	PWR	8/7/2017	COMPAL	EMI request to mount 0.1uF to PC208	to change PC208 to EMI@ 0.1uF	

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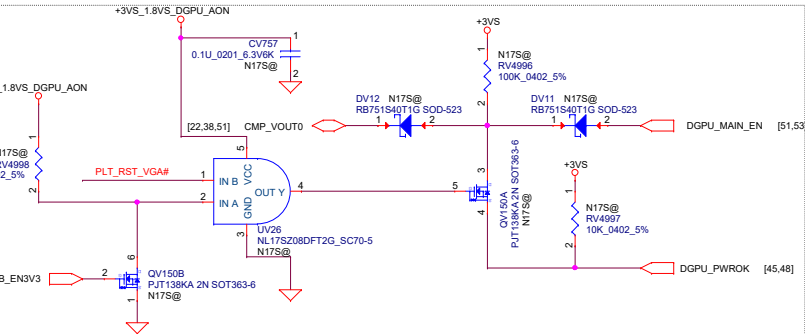
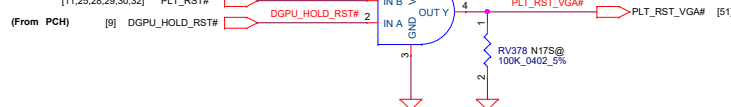
PCIE CLK

PCIE X4 Bus

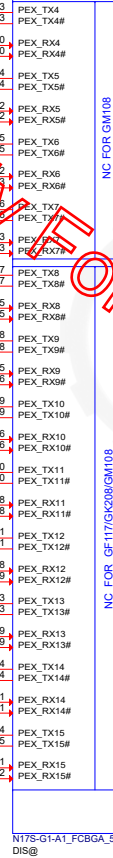
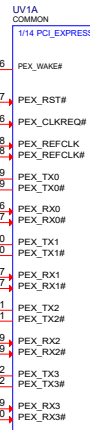
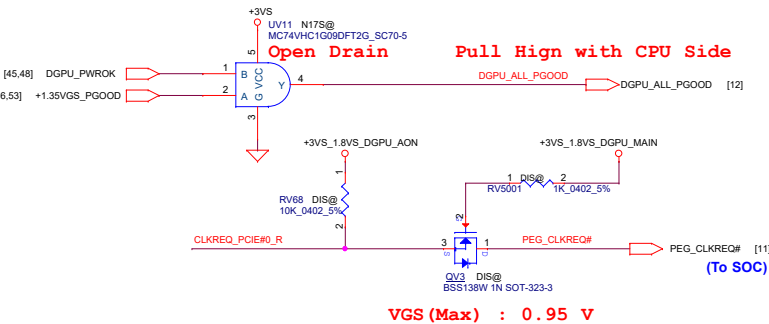


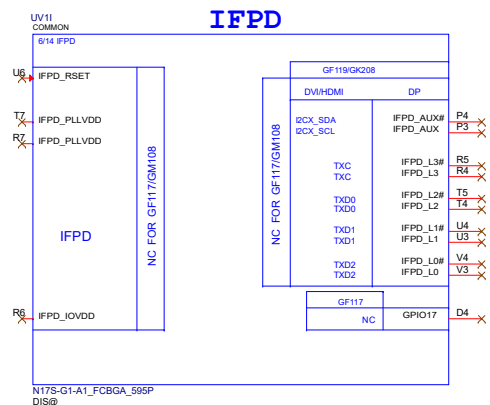
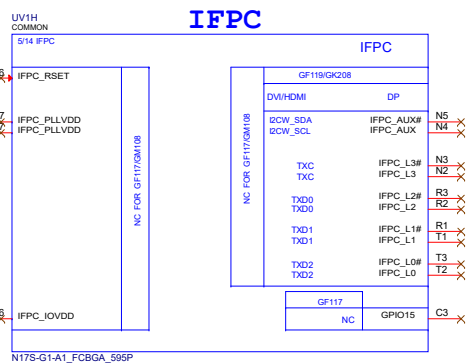
Reset Control

1.8V AND GATE

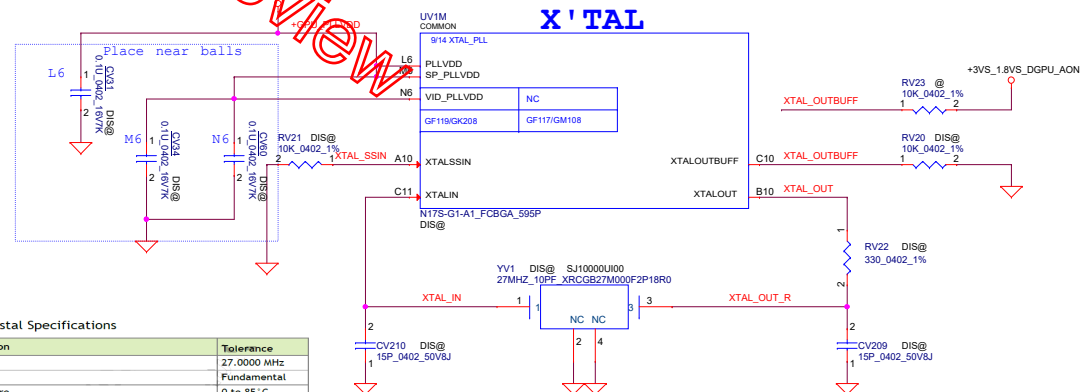
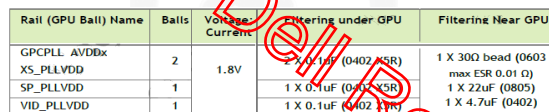
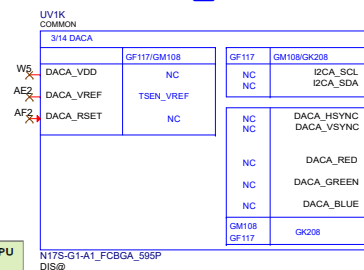


CLK_REQ





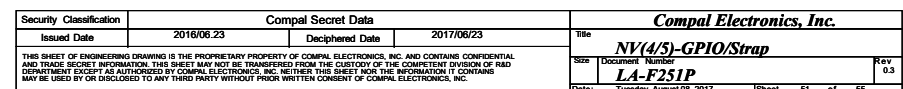
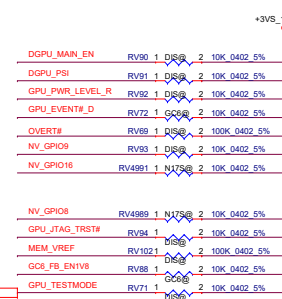
Note: IFPC/V/E/F interface are XVDDs pin for N17S GPU, and connect them to NVVDD power for improving NVVDD power ball routing

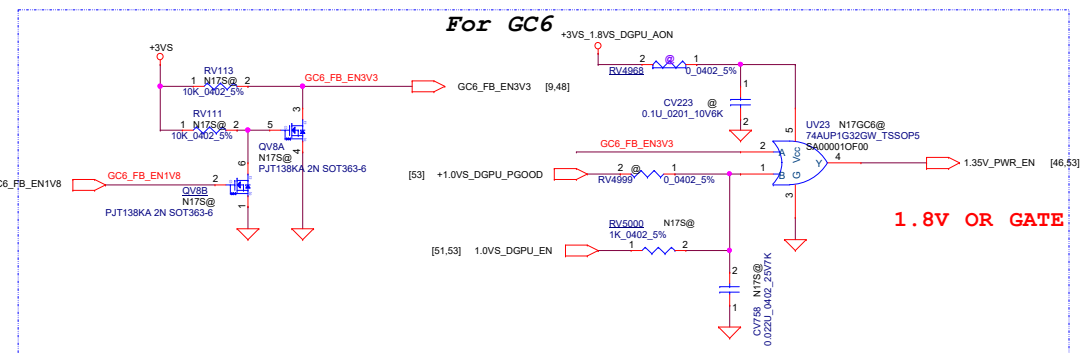


Parameter/Description	Tolerance
Nominal Frequency	27,0000 MHz
Oscillation Type	Fundamental
Operating Temperature	0 to 85 °C
Absolute accuracy with respect to frequency at room temperature (25 °C)	± 30 ppm
Variation over temperature range (From 0 degrees C to 70 degrees C)	± 30 ppm
Variation over time (typically 1 year)	± 5 ppm

Note: Crystal load capacitors should have 5% accuracy for best result; the value of the capacitors should be chosen according to manufacturer's specification.

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7.1.8 CKE* Signal

The diagram illustrates the timing for a GDDR5 Single Load operation. It features three main signal lines: GPU, FBVDDQ, and CKE. The GPU signal is shown as a square wave. The FBVDDQ signal is shown as a square wave with a 10 kΩ resistor connected to it. The CKE signal is shown as a square wave with a 10 kΩ resistor connected to it. The timing is defined by the following parameters:

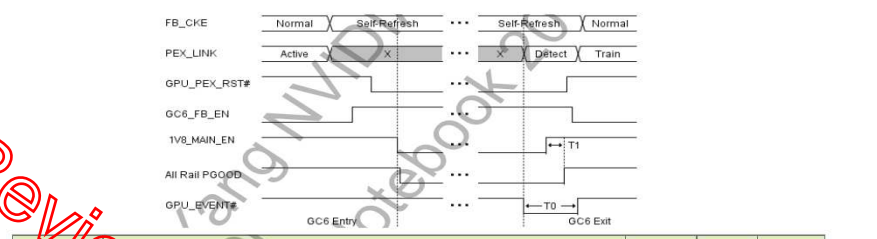
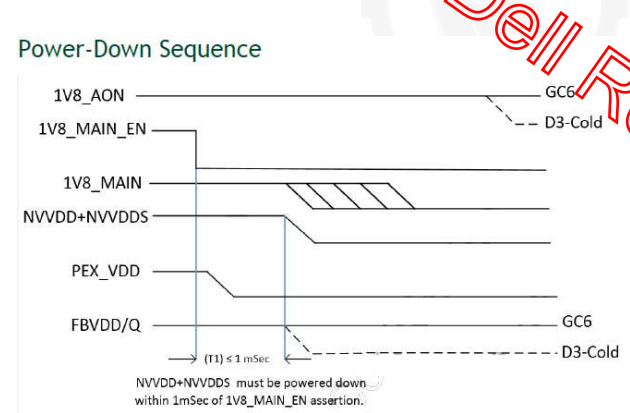
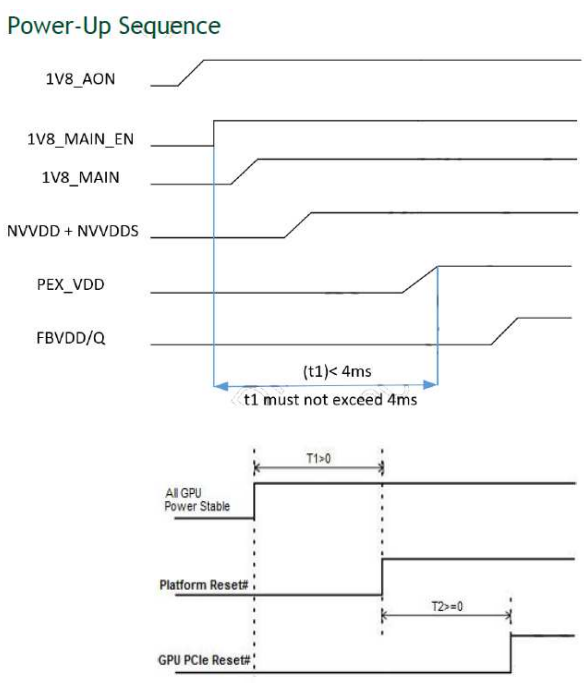
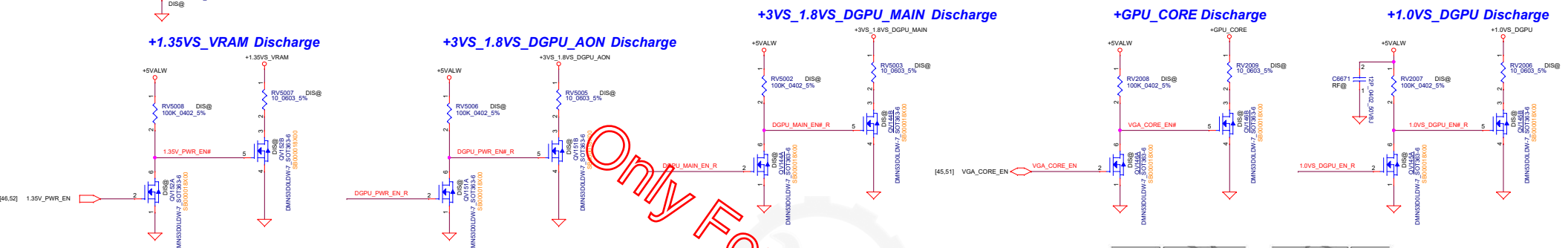
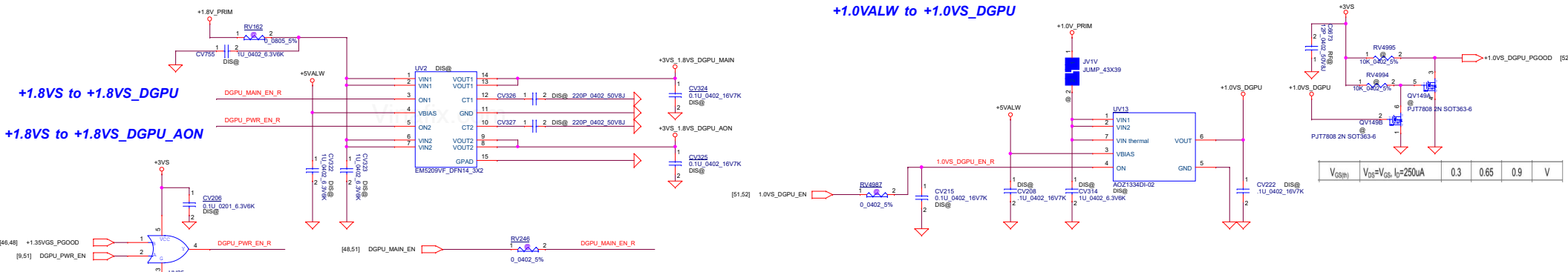
- GPU**: The signal source for the GPU.
- FBVDDQ**: The signal source for the FBVDDQ, connected to the GPU via a 10 kΩ resistor.
- CKE1***: The signal source for the CKE1* signal, connected to the GPU via a 10 kΩ resistor.
- CKE0***: The signal source for the CKE0* signal, connected to the GPU via a 10 kΩ resistor.
- GDDR5**: The memory device, shown as a block with two inputs: CKE1* and CKE0*.
- 1 chip in x32 mode**: The memory device is configured in a single chip in x32 mode.
- Single Load**: The memory device is configured for a single load operation.

7.1.7.3 RSI™ Signal

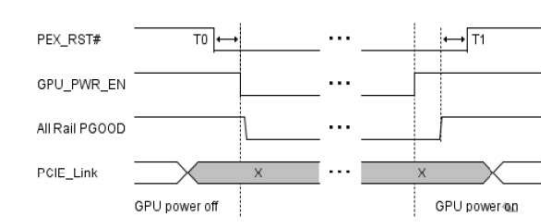
Figure 7-3. Reset Signal Connection

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 30Q bead (0603; max ESR 10 mΩ)
FBB_PLL_AVDD	1			1 X 22uF (0805)
FB_REFPLL_AVDD	1	1.8V	0.1uF (0402 X5R)	

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Symbol	Description	Min	Max	Units
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	1V8_MAIN_EN assertion to all power rails up and stable	0.04	4	ms



Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

Figure 8.4 Cold Reset Sequence Requirement for Optimus

Memory Partition A

Table 7-4. GDDR5 Mode H Mapping

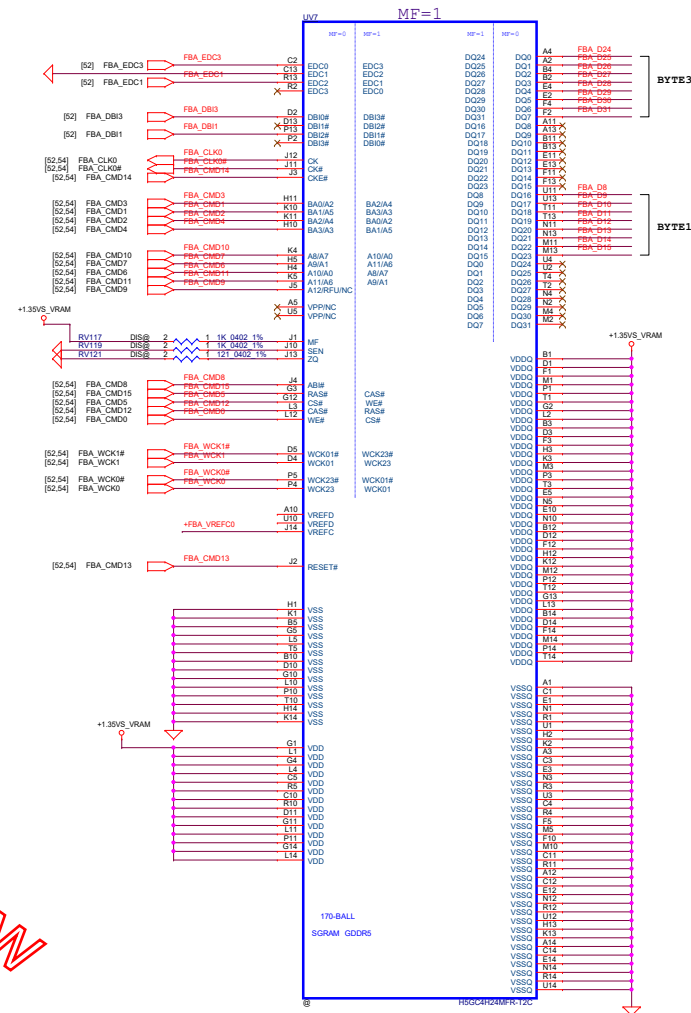
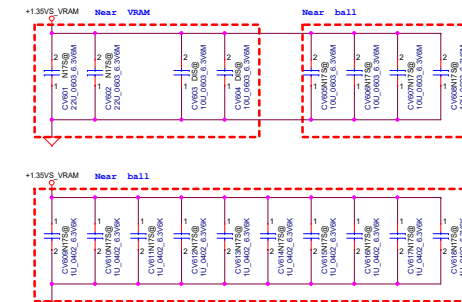
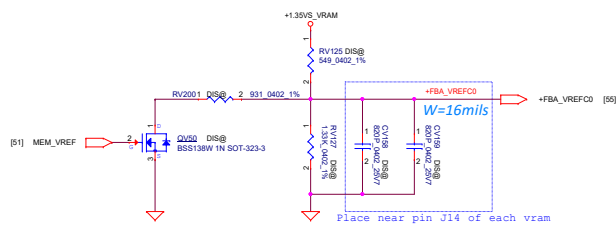
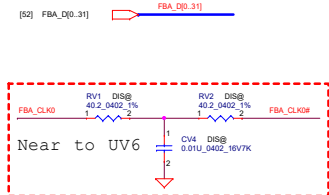
GB2-64, GB2-64, GB4-128	Channel 0...31	GB2-64, GB2-64, GB4-128	Channel 1 32...63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA0	CMD17	A3_BA3
CMD2	A4_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	R5T*	CMD29	R5T*
CMD14	CKE*	CMD30	CKE*
CMD15	CA5*	CMD31	CA5*
GB2-64, GB2-64, GB4-128 Channel 0 & 1			
CMD32	Hot_unused		
CMD33*	Hot_unused		
CMD34	DEBUG0*		
CMD35	DEBUG1*		

Notes:

- Hot available in GB2-64 and GB2-64 packages.
- GPU debug pins not connected to JTAG, see section 7.1.1.3.

Notes:

1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to URAM. See section 7.1.13.



Memory Partition B

Table 7-4. GDDR5 Mode H Mapping

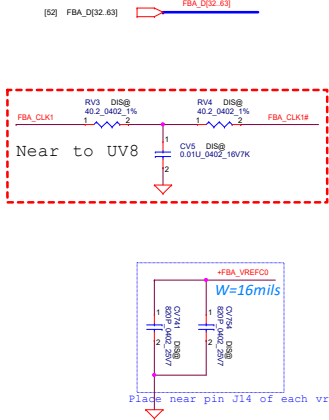
GB2-64, GB28-64, GB48-128	Channel 0 0..31	GB2-64, GB28-64, GB48-128	Channel 1 32..63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB*	CMD24	AB*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	RS1*	CMD29	RS1*
CMD14	CKE*	CMD30	CKE*
CMD15	CA5*	CMD31	CA5*

GB2-64, GB28-64, GB48-128 Channel 0 & 1

CMD32	Not used
CMD33	Not used
CMD34	DEBUG?
CMD35	DEBUG?

Notes:

- Not available in GB2-64 and GB28-64 packages.
- GPU debug pins not connected to DRAM, see section 7.1.13.



Place near pin J14 of each vram

